

BLF174XR; BLF174XRS

Power LDMOS transistor

Rev. 1 — 25 June 2013

Product data sheet

1. Product profile

1.1 General description

A 600 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 128 MHz band.

Table 1. Application information

Test signal	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
CW	108	50	600	28.5	74
pulsed RF	108	50	600	29	73

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 128 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

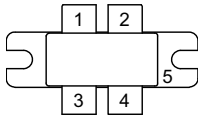
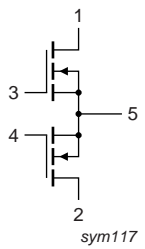
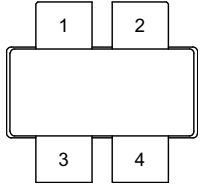
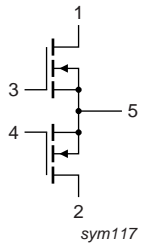
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF174XR (SOT1214A)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF174XRS (SOT1214B)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLF174XR	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1214A
BLF174XRS	-	earless flanged ceramic package; 4 leads	SOT1214B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[1]	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 150\text{ °C}$	[1][2] 0.18	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 2.75\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 275\text{ mA}$	1.25	1.7	2.25	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	38	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 9.625\text{ A}$	-	0.15	-	Ω

Table 7. AC characteristics

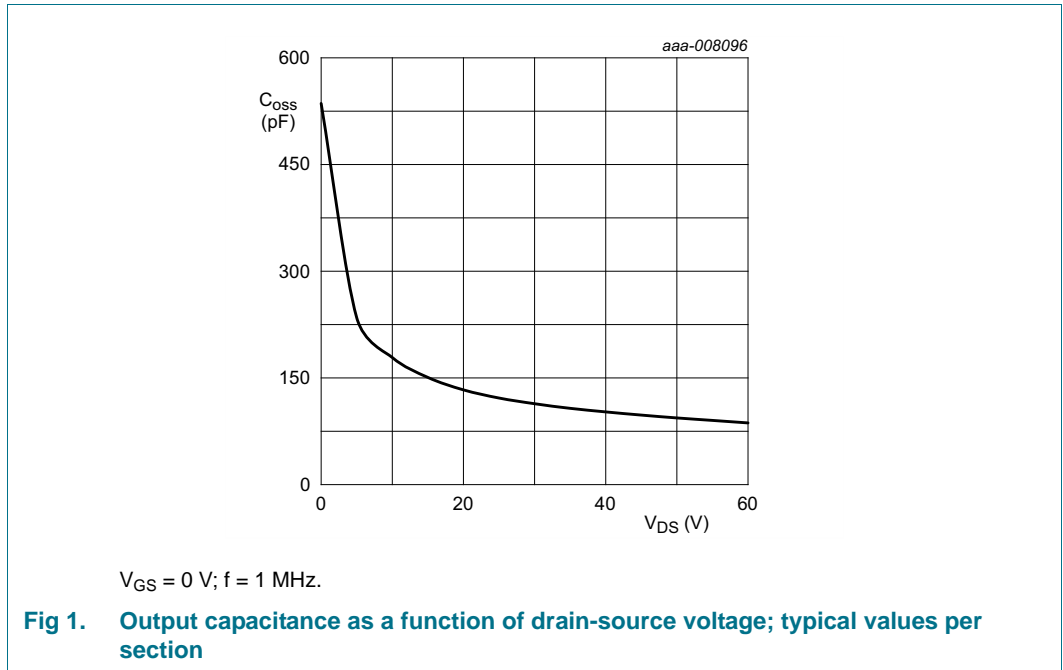
$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	2.4	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	210	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	94	-	pF

Table 8. RF characteristics

Test signal: CW; $f = 108\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$; $I_{Dq} = 100\text{ mA}$; $T_{case} = 25\text{ °C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 600\text{ W}$	27.0	28.5	-	dB
RL_{in}	input return loss	$P_L = 600\text{ W}$	-	-21	-13	dB
η_D	drain efficiency	$P_L = 600\text{ W}$	70	74	-	%



7. Test information

7.1 Ruggedness in class-AB operation

The BLF174XR and BLF174XRS are capable of withstanding a load mismatch corresponding to $V_{SWR} > 65 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}; P_L = 600\text{ W}$ pulsed; $f = 108\text{ MHz}.$

7.2 Impedance information

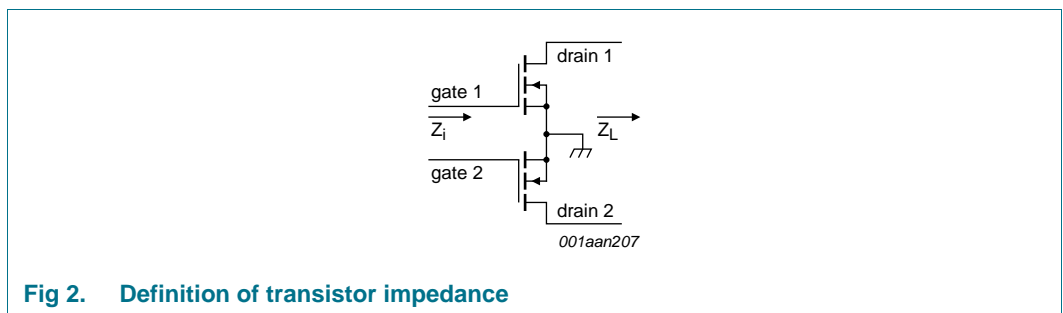
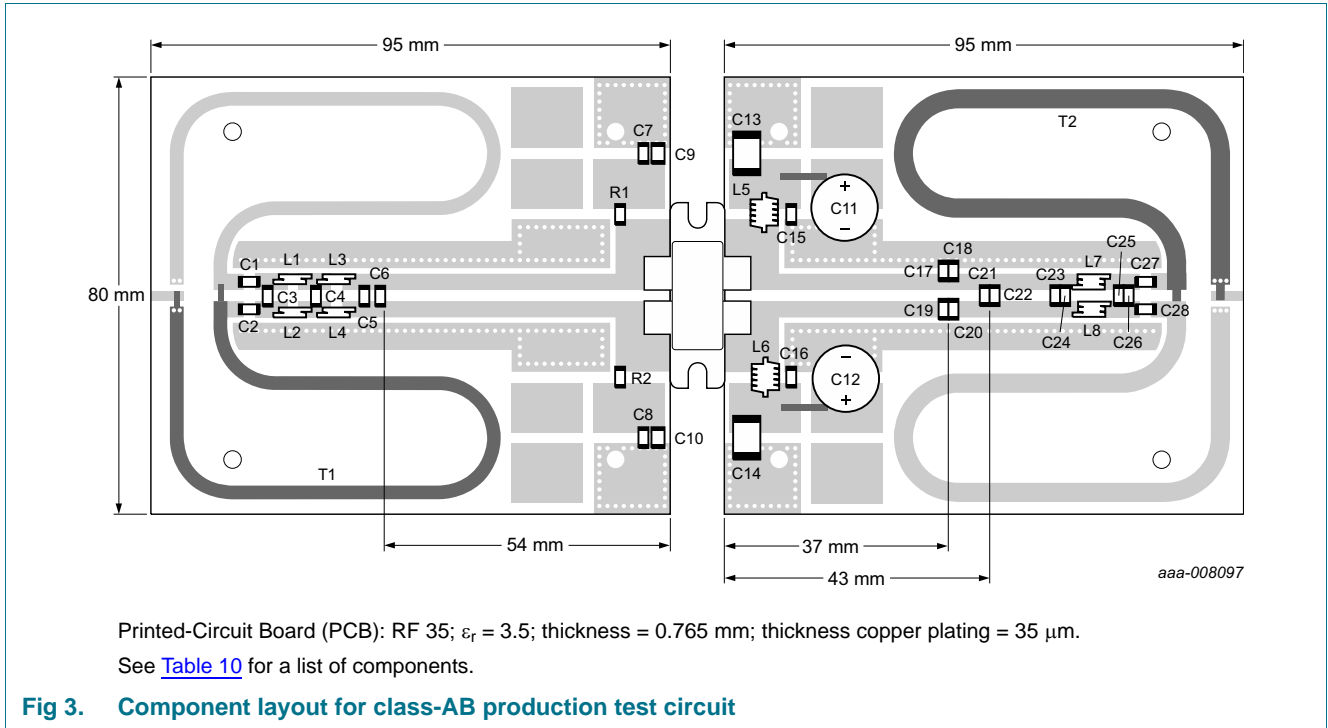


Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at $V_{DS} = 50\text{ V}$ and $P_L = 600\text{ W}.$

f (MHz)	Z_i (Ω)	Z_L (Ω)
108	$4.66 - j12.04$	$6.47 + j1.16$

7.3 Test circuit



Printed-Circuit Board (PCB): RF 35; $\epsilon_r = 3.5$; thickness = 0.765 mm; thickness copper plating = 35 μm .

See [Table 10](#) for a list of components.

Fig 3. Component layout for class-AB production test circuit

Table 10. List of components

For test circuit see [Figure 3](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	910 pF	[1]
C3	multilayer ceramic chip capacitor	51 pF	[2]
C4	multilayer ceramic chip capacitor	43 pF	[1]
C5	multilayer ceramic chip capacitor	100 pF	[1]
C6	multilayer ceramic chip capacitor	75 pF	[1]
C7, C8, C15, C16	multilayer ceramic chip capacitor	820 pF	[1]
C9, C10	multilayer ceramic chip capacitor	4.7 μF , 100 V	TDK C5750X7R2A475KT
C11, C12	electrolytic capacitor	470 μF , 63 V	
C13, C14	multilayer ceramic chip capacitor	4.7 μF , 100 V	
C17, C18, C19, C20	multilayer ceramic chip capacitor	39 pF	[1]
C21, C23	multilayer ceramic chip capacitor	22 pF	[1]
C22	multilayer ceramic chip capacitor	15 pF	[1]
C24	multilayer ceramic chip capacitor	20 pF	[1]
C25, C26	multilayer ceramic chip capacitor	27 pF	[1]
C27, C28	multilayer ceramic chip capacitor	1 nF	[2]
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 3.6 mm, length = 1.8 mm	

Table 10. List of components ...continued
For test circuit see [Figure 3](#).

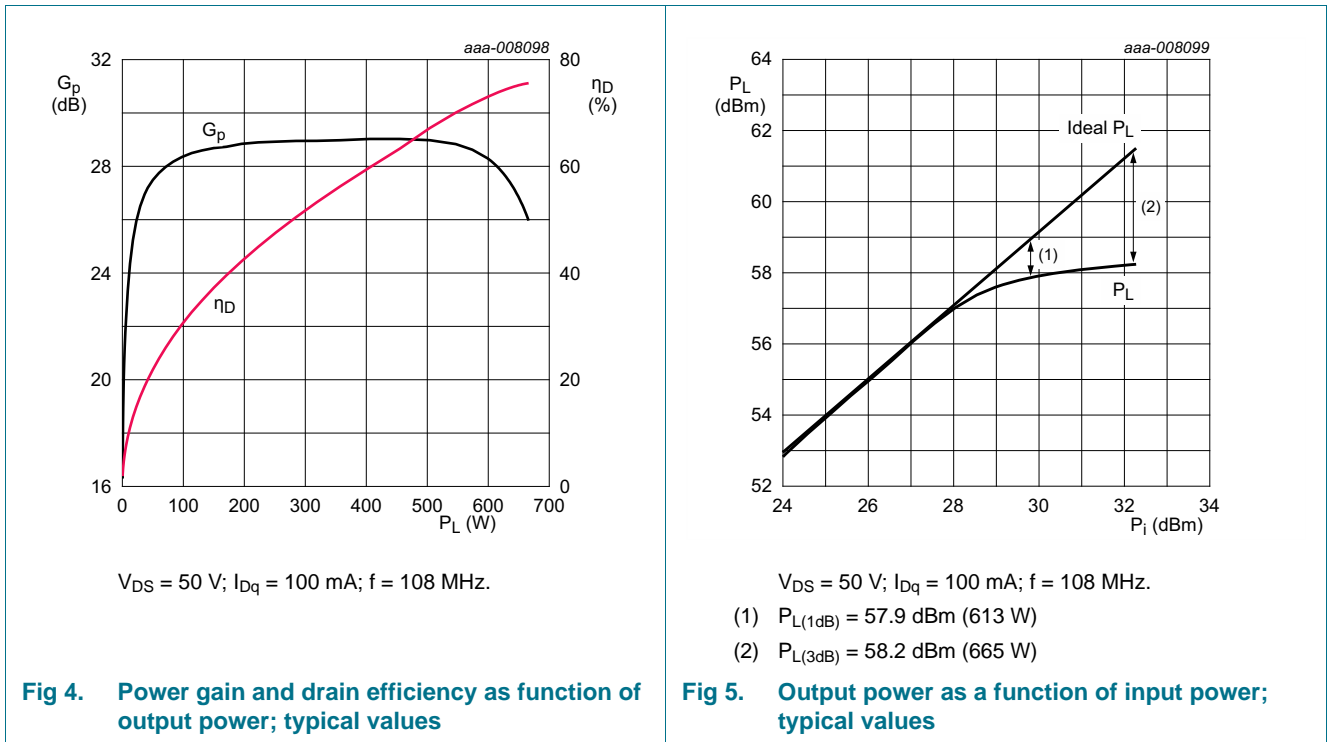
Component	Description	Value	Remarks
L5, L6	5.5 turn 0.8 mm copper wire	D = 4.4 mm, length = 5.2 mm	
L7, L8	1.5 turn 1.5 mm copper wire	D = 6.5 mm, length = 3.2 mm	
R1, R2	resistor	10.0 Ω	SMD 1206
T1	semi rigid coax	25 Ω, 160 mm	Micro-Coax UT-090C-25
T2	semi rigid coax	25 Ω, 160 mm	Micro-Coax UT-141C-25

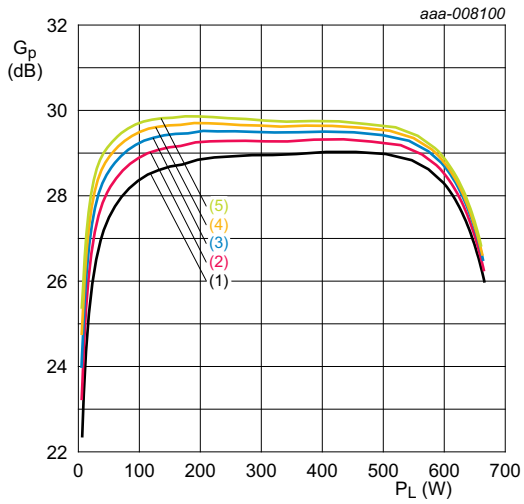
- [1] American Technical Ceramics type 800B or capacitor of same quality.
- [2] American Technical Ceramics type 100B or capacitor of same quality.

7.4 Graphical data

The following figures are measured in a class-AB production test circuit.

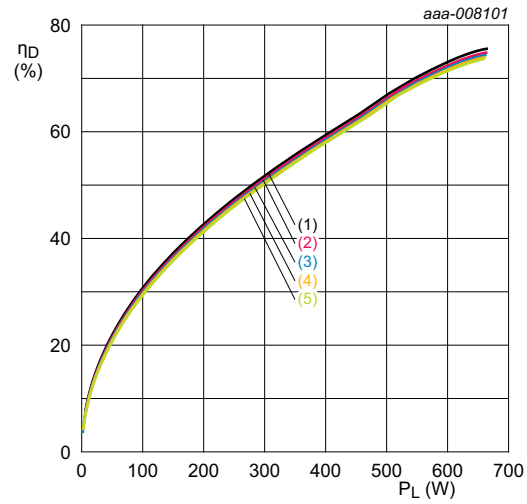
7.4.1 1-Tone CW





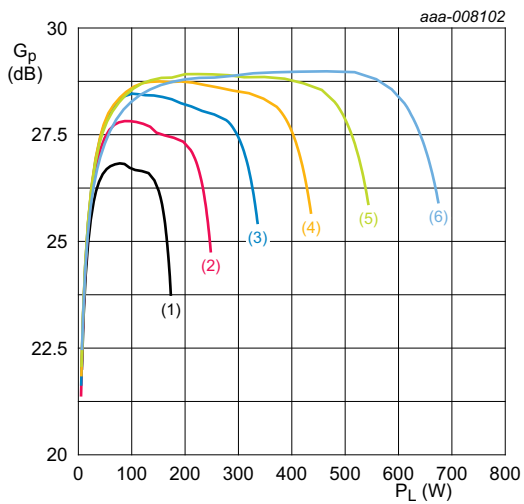
- $V_{DS} = 50\text{ V}; f = 108\text{ MHz.}$
- (1) $I_{Dq} = 100\text{ mA}$
 - (2) $I_{Dq} = 200\text{ mA}$
 - (3) $I_{Dq} = 300\text{ mA}$
 - (4) $I_{Dq} = 400\text{ mA}$
 - (5) $I_{Dq} = 500\text{ mA}$

Fig 6. Power gain as a function of output power; typical values



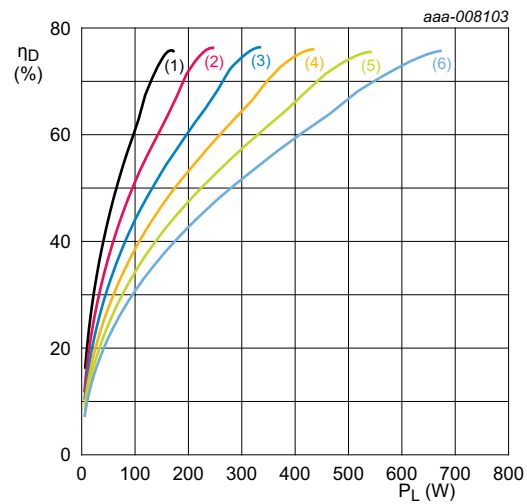
- $V_{DS} = 50\text{ V}; f = 108\text{ MHz.}$
- (1) $I_{Dq} = 100\text{ mA}$
 - (2) $I_{Dq} = 200\text{ mA}$
 - (3) $I_{Dq} = 300\text{ mA}$
 - (4) $I_{Dq} = 400\text{ mA}$
 - (5) $I_{Dq} = 500\text{ mA}$

Fig 7. Drain efficiency as a function of output power; typical values



- $I_{Dq} = 100\text{ mA}; f = 108\text{ MHz.}$
- (1) $V_{DS} = 25\text{ V}$
 - (2) $V_{DS} = 30\text{ V}$
 - (3) $V_{DS} = 35\text{ V}$
 - (4) $V_{DS} = 40\text{ V}$
 - (5) $V_{DS} = 45\text{ V}$
 - (6) $V_{DS} = 50\text{ V}$

Fig 8. Power gain as a function of output power; typical values



- $I_{Dq} = 100\text{ mA}; f = 108\text{ MHz.}$
- (1) $V_{DS} = 25\text{ V}$
 - (2) $V_{DS} = 30\text{ V}$
 - (3) $V_{DS} = 35\text{ V}$
 - (4) $V_{DS} = 40\text{ V}$
 - (5) $V_{DS} = 45\text{ V}$
 - (6) $V_{DS} = 50\text{ V}$

Fig 9. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 4 leads

SOT1214A

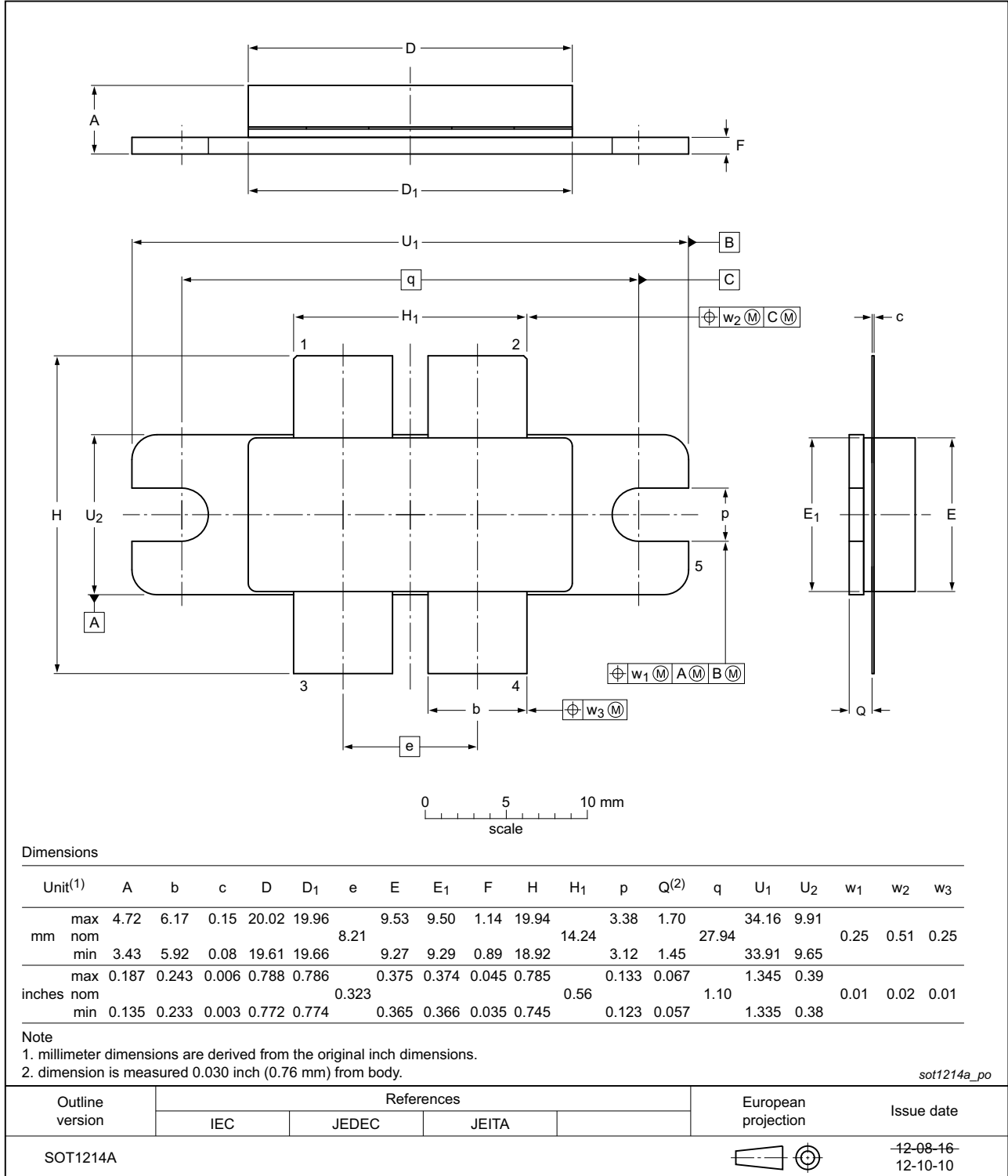


Fig 10. Package outline SOT1214A

Earless flanged ceramic package; 4 leads

SOT1214B

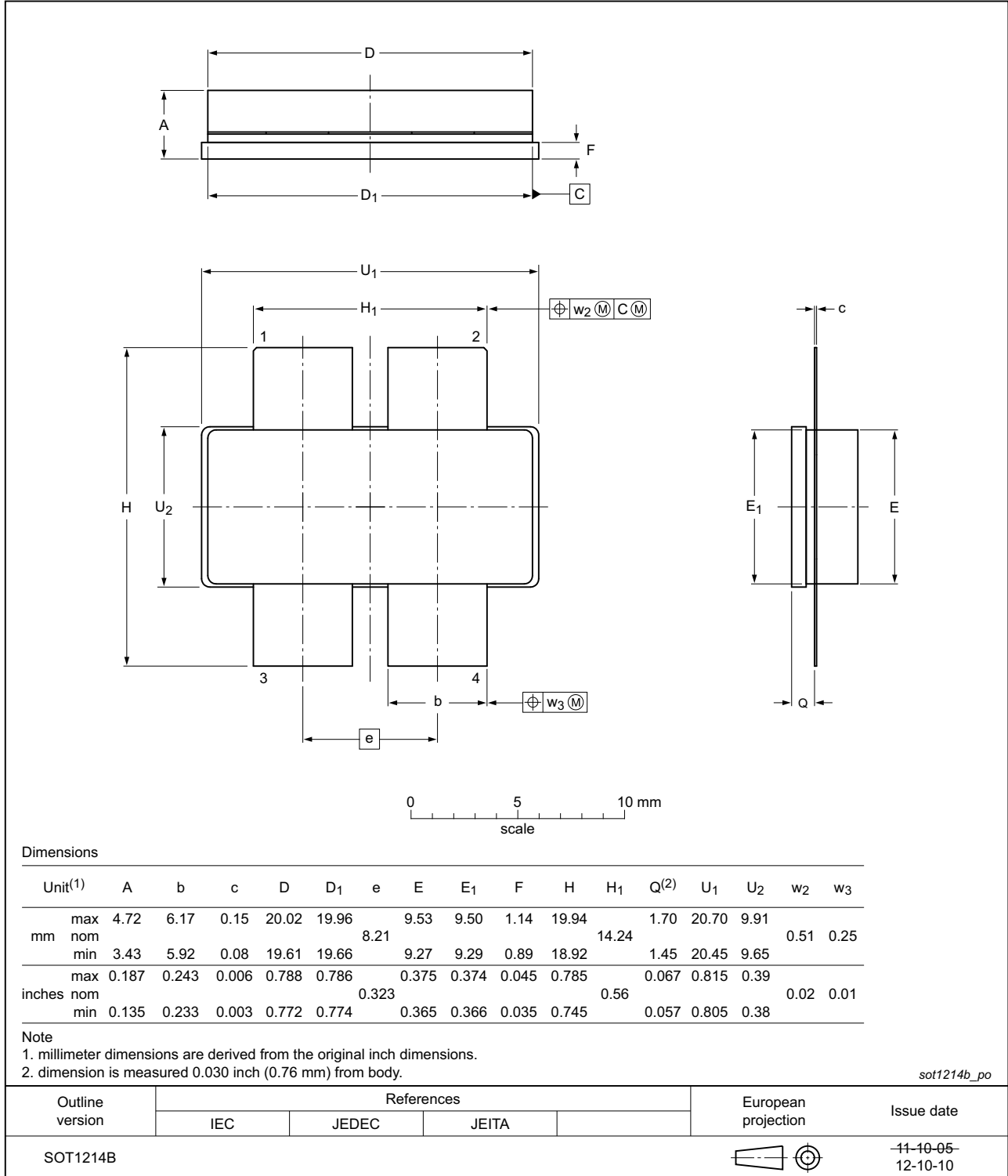


Fig 11. Package outline SOT1214B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
XR	eXtremely Rugged

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF174XR_BLF174XRS v.1	20130625	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	3
7	Test information	4
7.1	Ruggedness in class-AB operation	4
7.2	Impedance information	4
7.3	Test circuit	5
7.4	Graphical data	6
7.4.1	1-Tone CW	6
8	Package outline	8
9	Handling information	10
10	Abbreviations	10
11	Revision history	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12
13	Contact information	12
14	Contents	13

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