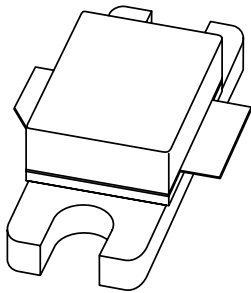


# DATA SHEET



## **BLF1820-40** UHF power LDMOS transistor

Preliminary specification

2001 Aug 10

# UHF power LDMOS transistor

# BLF1820-40

### FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Designed for broadband operation (1.8 to 2 GHz)
- Internal input and output matching for high gain and efficiency
- Improved linearity at backoff levels.

### APPLICATIONS

- Common source class-AB operation for PCN and PCS applications in the 1800 to 2000 MHz frequency range
- Suitable for GSM, Edge, CDMA and WCDMA applications.

### DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistors encapsulated in a 2-lead SOT608A flange package with a ceramic cap. The common source is connected to the mounting flange.

### PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

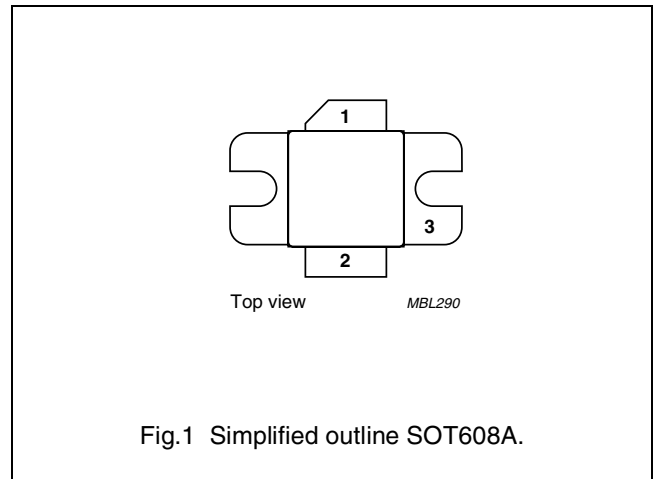


Fig.1 Simplified outline SOT608A.

### QUICK REFERENCE DATA

RF performance at  $T_h = 25\text{ °C}$  in a common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	PL (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_{im}$ (dBc)
Two-tone, class-AB	$f_1 = 2000; f_2 = 2000.1$	26	40 (PEP)	>10.5	>30	$\leq -25$

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage	–	65	V
$V_{GS}$	gate-source voltage	–	$\pm 15$	V
$I_D$	DC drain current	–	5	A
$T_{stg}$	storage temperature	–65	+150	°C
$T_j$	junction temperature	–	200	°C

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_h = 25\text{ °C}$ , $P_{tot} = 152\text{ W}$ , note 1	2.3	K/W

## Note

1. Determined under specified RF operating conditions.

## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = 1\text{ mA}$	65	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 90\text{ mA}$	–	5	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = 26\text{ V}$	–	–	5	$\mu\text{A}$
$I_{DSX}$	on-state drain current	$V_{GS} = V_{GS\ th} + 9\text{ V}$ ; $V_{DS} = 10\text{ V}$	13	14	–	A
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 15\text{ V}$ ; $V_{DS} = 0$	–	–	30	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 3\text{ A}$	–	2.5	–	S
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = V_{GS\ th} + 9\text{ V}$ ; $I_D = 3\text{ A}$	–	0.25	–	$\Omega$
$C_{rSS}$	feedback capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\text{ V}$ ; $f = 1\text{ MHz}$	–	1.7	–	pF

## APPLICATION INFORMATION

RF performance in a common source class-AB circuit.  $T_h = 25\text{ °C}$ ;  $R_{th\ j-h} = 1.15\text{ K/W}$ , unless otherwise specified.

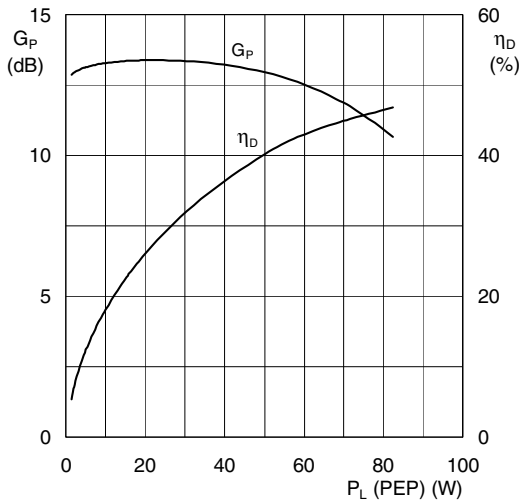
MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$I_{DQ}$ (mA)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_{im}$ (dBc)
Two-tone, class-AB	$f_1 = 2000$ ; $f_2 = 2000.1$	26	300	40 (PEP)	>10.5	>30	$\leq -25$

## Ruggedness in class-AB operation

The BLF1820-40 is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 26\text{ V}$ ;  $I_{DQ} = 300\text{ mA}$ ;  $P_L = 40\text{ W}$ ;  $f = 2000\text{ MHz}$ .

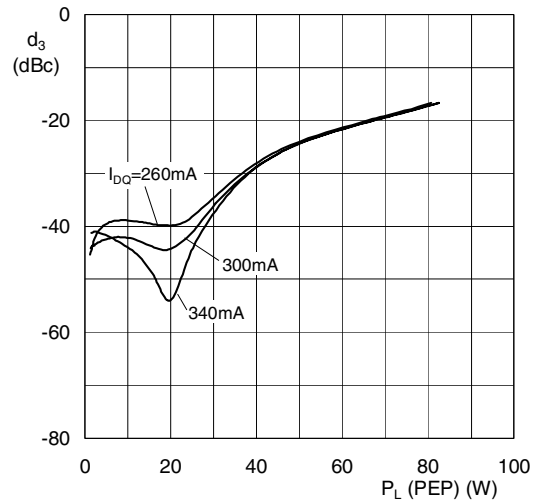
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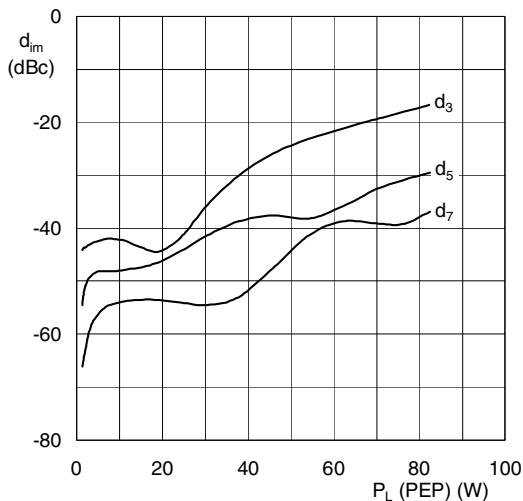
V<sub>DS</sub> = 26 V; I<sub>DQ</sub> = 300 mA; f<sub>1</sub> = 2000 MHz; f<sub>2</sub> = 2000.1 MHz.

Fig.2 Power gain and efficiency as functions of peak envelope load power, typical values.



V<sub>DS</sub> = 26 V; f<sub>1</sub> = 2000 MHz; f<sub>2</sub> = 2000.1 MHz.

Fig.3 Intermodulation distortion as a function of peak envelope load power, typical values.

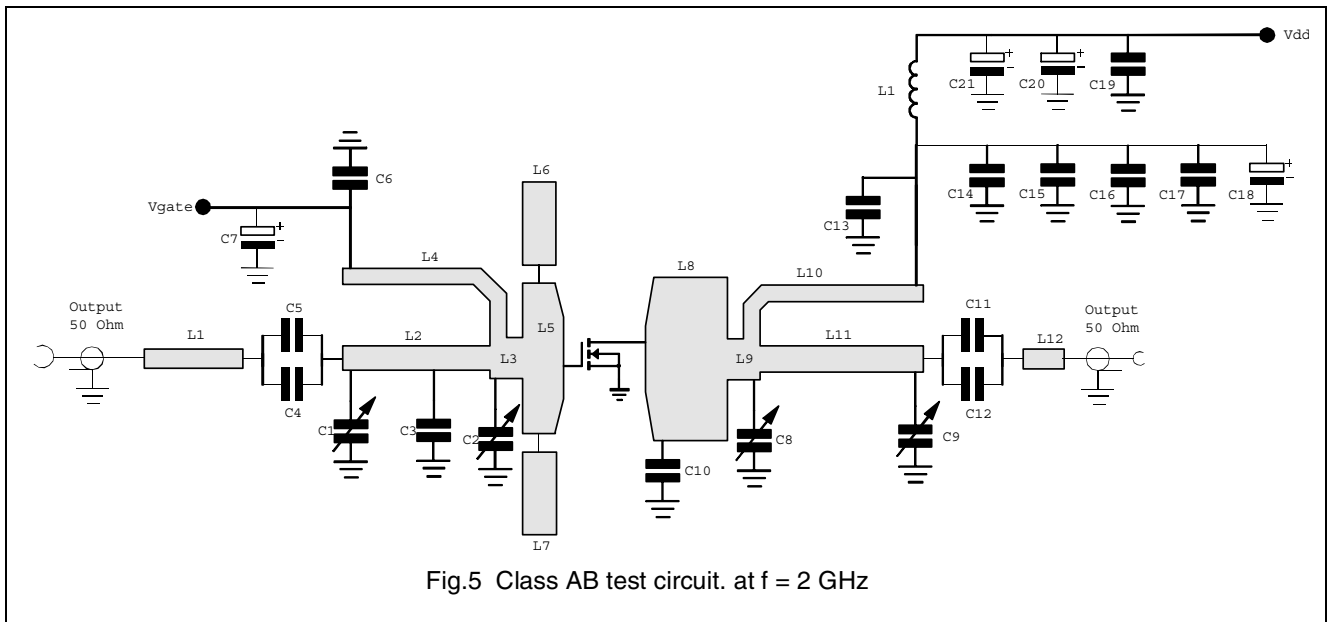


V<sub>DS</sub> = 26 V; I<sub>DQ</sub> = 300 mA; f<sub>1</sub> = 2000 MHz; f<sub>2</sub> = 2000.1 MHz.

Fig.4 Intermodulation distortion as a function of peak envelope load power, typical values.

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## List of components

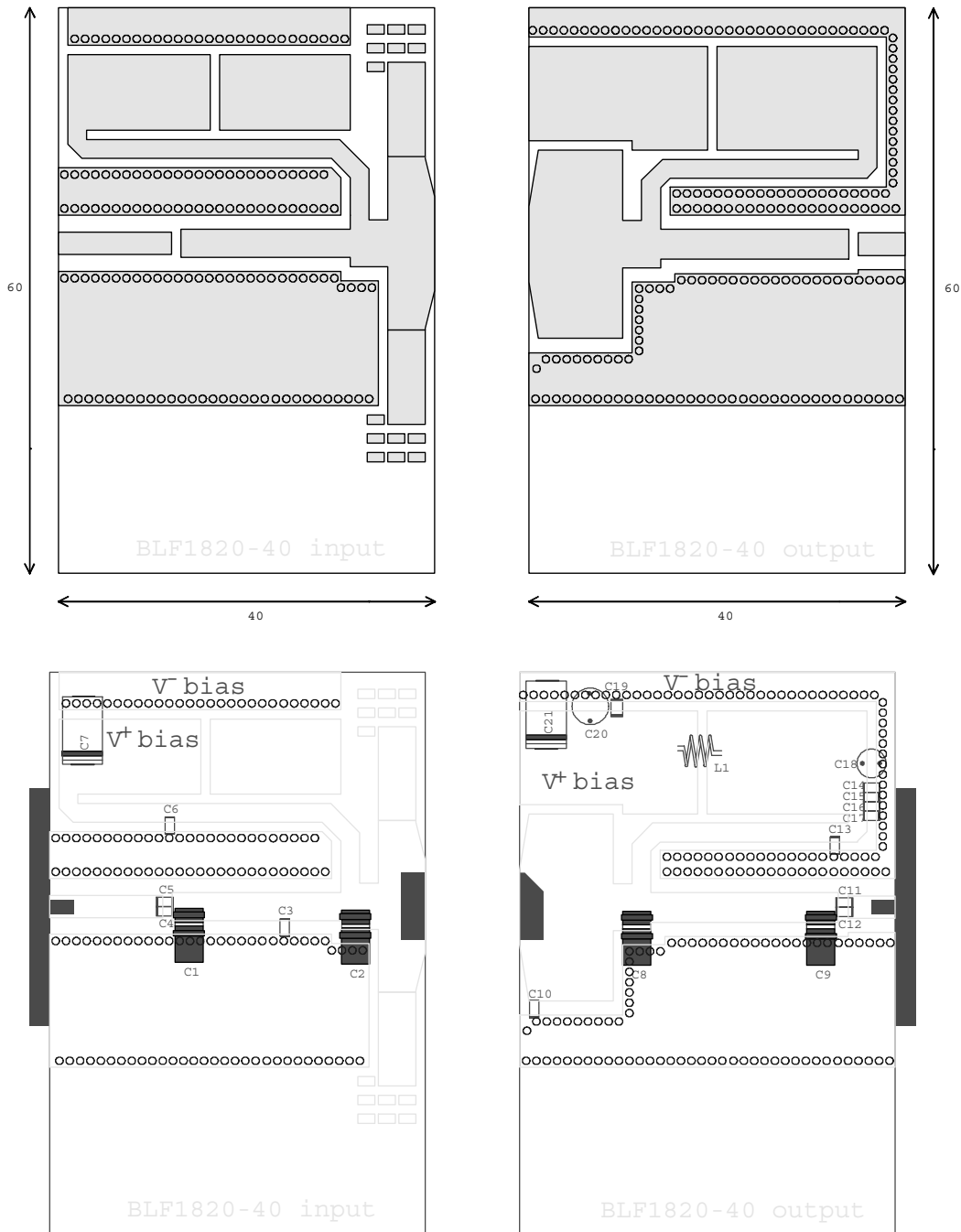
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C8, C9	Tekelec trimmer; type 37271	0.6 to 4.5 pF		
C3	multilayer ceramic chip capacitor; note 1	1.5 pF		
C4, C5, C11, C12	multilayer ceramic chip capacitor; note 1	6.8 pF		
C6, C13	multilayer ceramic chip capacitor; note 2	12 pF		
C7, C20, C21	electrolytic capacitor	100 $\mu$ F; 63 V		2222 037 58101
C10	multilayer ceramic chip capacitor; note 1	1 pF		
C14	multilayer ceramic chip capacitor; note 1	10 pF		
C15	multilayer ceramic chip capacitor; note 1	20 pF		
C16	multilayer ceramic chip capacitor; note 1	120 pF		
C17	Philips SMD capacitor	100 nF		
C18	electrolytic capacitor	47 $\mu$ F; 35 V		
C19	multilayer ceramic chip capacitor; note 2	6.8 nF		
L1, L12	stripline; note 3	50 $\Omega$	2.4 x 12 mm	
L2	stripline; note 3	42.8 $\Omega$	3.0 x 18 mm	
L3, L9	stripline; note 3	29.4 $\Omega$	5.0 x 4.0 mm	
L4, L10	stripline; note 3		2.0 x 25 mm	
L5	stripline; note 3	9.7 $\Omega$	18.4 x 5.0 mm	
L6, L7	stripline; note 3			
L8	stripline; note 3	9.0 $\Omega$	211 x 10 mm	
L11	stripline; note 3	40.9 $\Omega$	3.2 x 20 mm	

## Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad Rogers 6006 printed-circuit board ( $\epsilon_r = 6.15$ ); thickness = 25 mils.

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Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board ( $\epsilon_r = 6.15$ ); thickness = 25 mils. The other side is unetched and serves as a ground plane.

Fig.6 Printed circuit board for 2 GHz test circuit.

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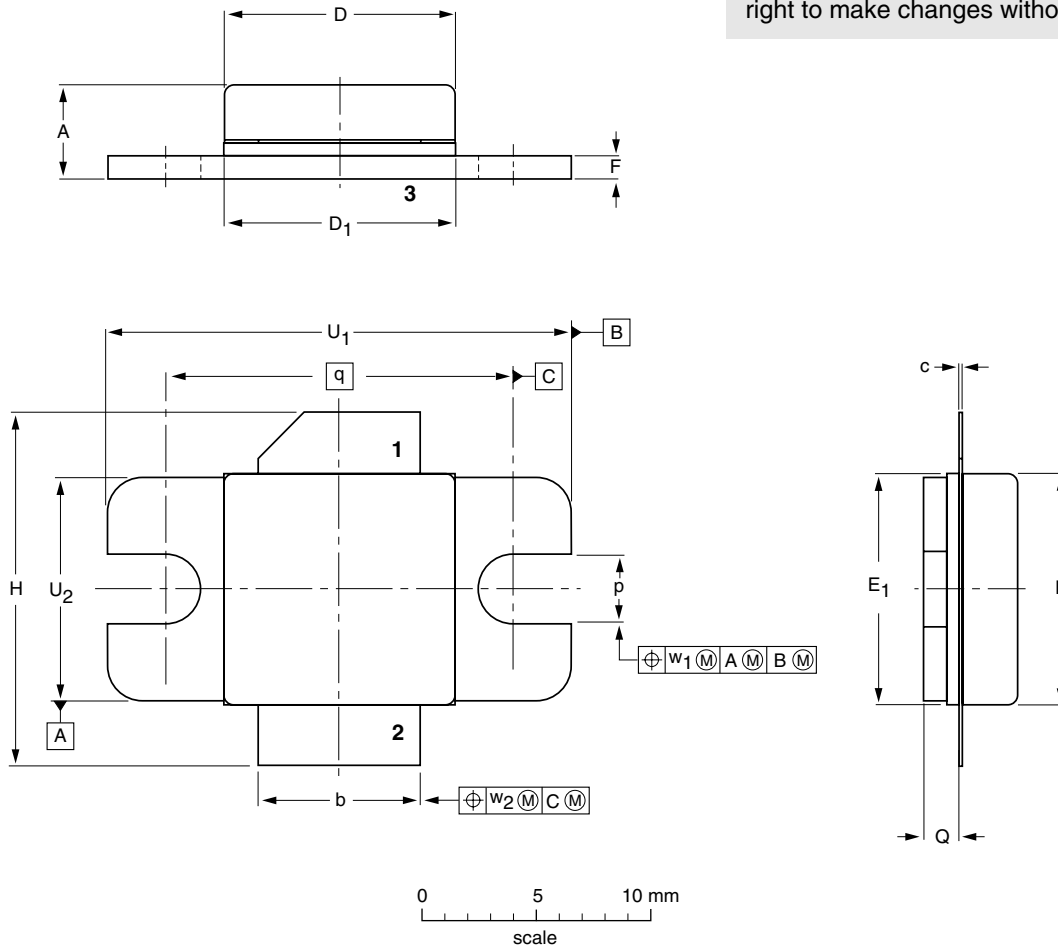
PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 2 leads

SOT608A

**Package under development**

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.75 3.73	7.24 6.99	0.15 0.10	10.29 9.98	10.29 10.03	10.29 9.98	10.29 10.03	1.14 0.89	15.75 14.73	3.43 3.18	1.70 1.35	15.24	20.45 20.19	9.91 9.65	0.25	0.51
inches	0.187 0.147	0.285 0.275	0.006 0.004	0.405 0.393	0.405 0.395	0.405 0.393	0.405 0.395	0.045 0.035	0.620 0.580	0.125 0.115	0.067 0.053	0.600	0.805 0.795	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT608A						01-02-02- 01-02-22

## UHF power LDMOS transistor

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.



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