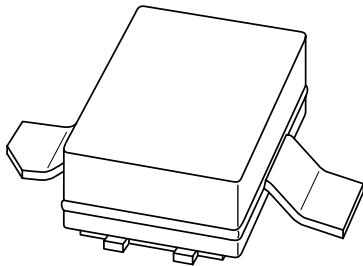


# DATA SHEET



**BLF2043**

**UHF power LDMOS transistor**

Product specification  
Supersedes data of 2002 Sep 10

2003 Feb 10

# UHF power LDMOS transistor

# BLF2043

## FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and  $I_{DQ}$  of 85 mA:
  - Output power = 10 W (PEP)
  - Gain = 12 dB
  - Efficiency = 36.5%
  - $d_{im} = -32$  dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (HF to 2200 MHz)
- No internal matching for broadband operation.

## APPLICATIONS

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the HF to 2200 MHz frequency range
- Broadcast drivers.

## DESCRIPTION

10 W LDMOS power transistor for base station applications at frequencies from HF to 2200 MHz.

## QUICK REFERENCE DATA

Typical RF performance at  $T_h = 25$  °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	PL (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_{im}$ (dBc)
CW, class-AB (2-tone)	$f_1 = 2000; f_2 = 2000.1$	26	10 (PEP)	12.5	36.5	-32

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

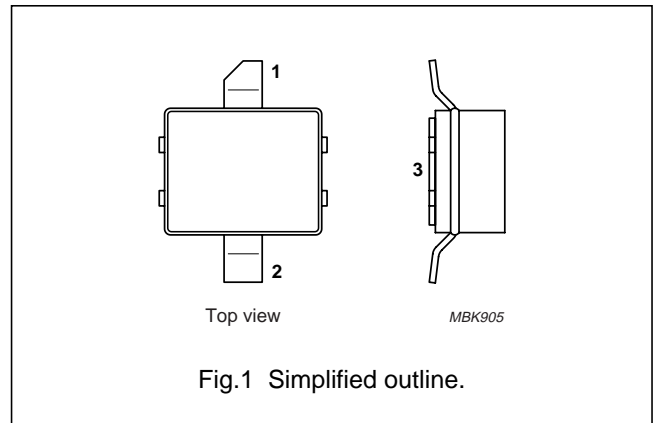
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	75	V
$V_{GS}$	gate-source voltage		–	±15	V
$I_D$	drain current (DC)		–	2.2	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		–	200	°C

### CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

## PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to mounting base



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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_{mb} = 25\text{ °C}$ ; note 1	9	K/W

## Note

1. Thermal resistance is determined under RF operating conditions.

## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = 0.2\text{ mA}$	65	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 20\text{ mA}$	4	–	5	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = 26\text{ V}$	–	–	1.5	$\mu\text{A}$
$I_{DSX}$	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}$ ; $V_{DS} = 10\text{ V}$	2.8	–	–	A
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 15\text{ V}$ ; $V_{DS} = 0$	–	–	40	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 0.75\text{ A}$	–	0.5	–	S
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 0.75\text{ A}$	–	1.2	–	$\Omega$
$C_{is}$	input capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\text{ V}$ ; $f = 1\text{ MHz}$	–	11	–	pF
$C_{os}$	output capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\text{ V}$ ; $f = 1\text{ MHz}$	–	9	–	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\text{ V}$ ; $f = 1\text{ MHz}$	–	0.5	–	pF

## APPLICATION INFORMATION

RF performance in a common source class-AB circuit.  $T_h = 25\text{ °C}$ ;  $R_{th\ mb-h} = 0.4\text{ K/W}$ , unless otherwise specified.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$I_{DQ}$ (mA)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_{im}$ (dBc)
CW, class-AB (2-tone)	$f_1 = 2000$ ; $f_2 = 2000.1$	26	85	10 (PEP)	>11.8	>33	$\leq -26$

## Ruggedness in class-AB operation

The BLF2043 is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 26\text{ V}$ ;  $f = 2000\text{ MHz}$  at rated load power.

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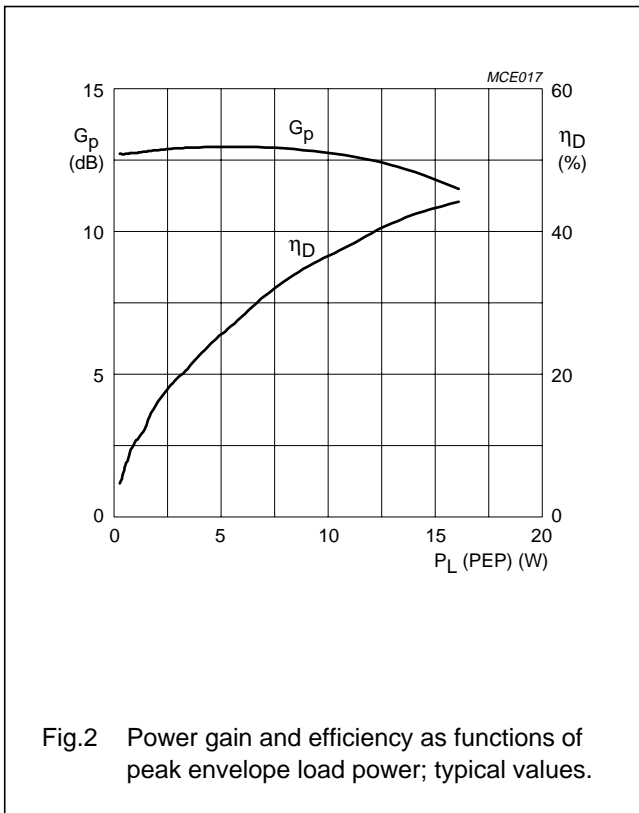


Fig.2 Power gain and efficiency as functions of peak envelope load power; typical values.

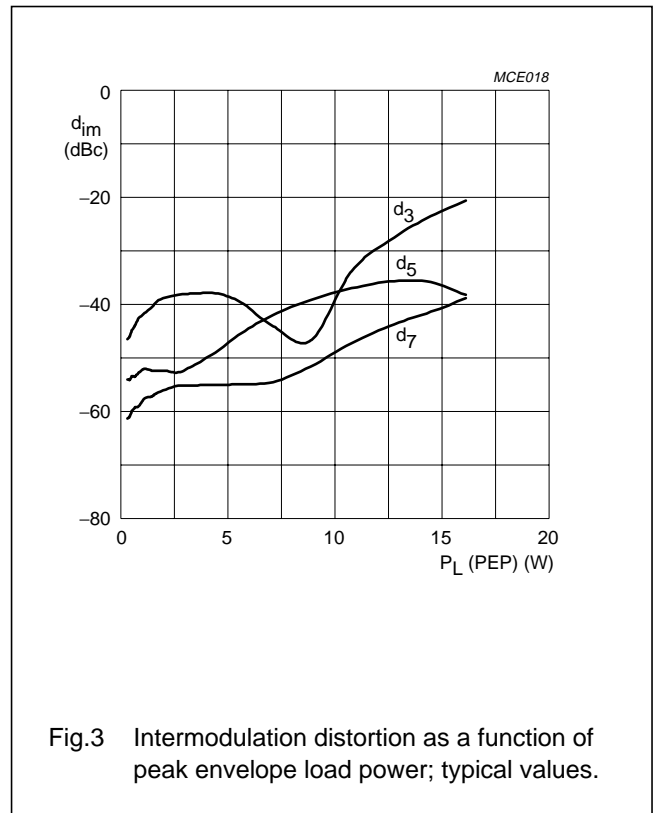


Fig.3 Intermodulation distortion as a function of peak envelope load power; typical values.

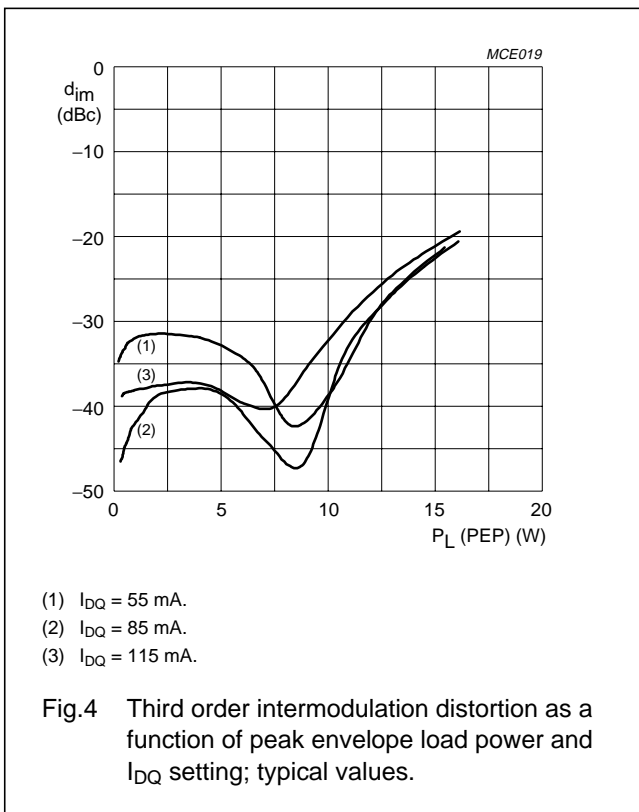
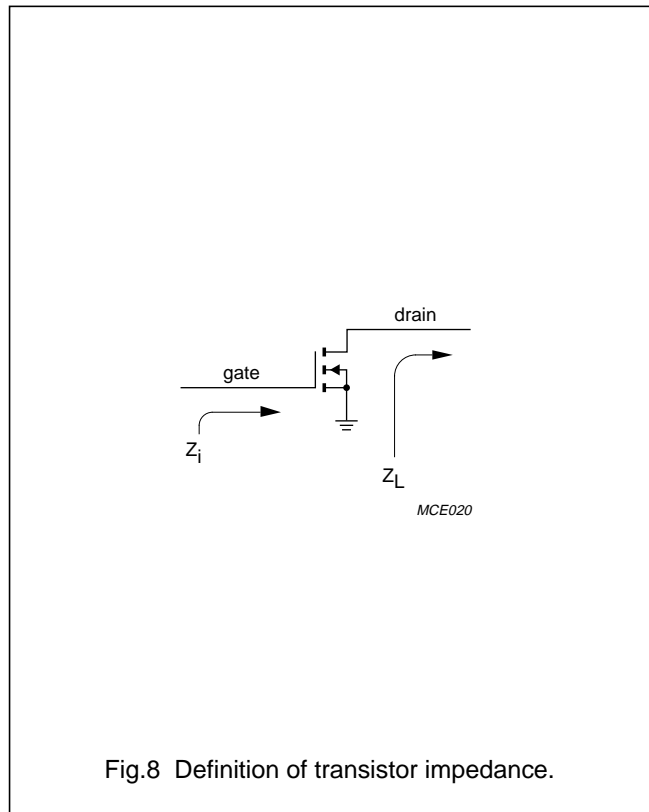
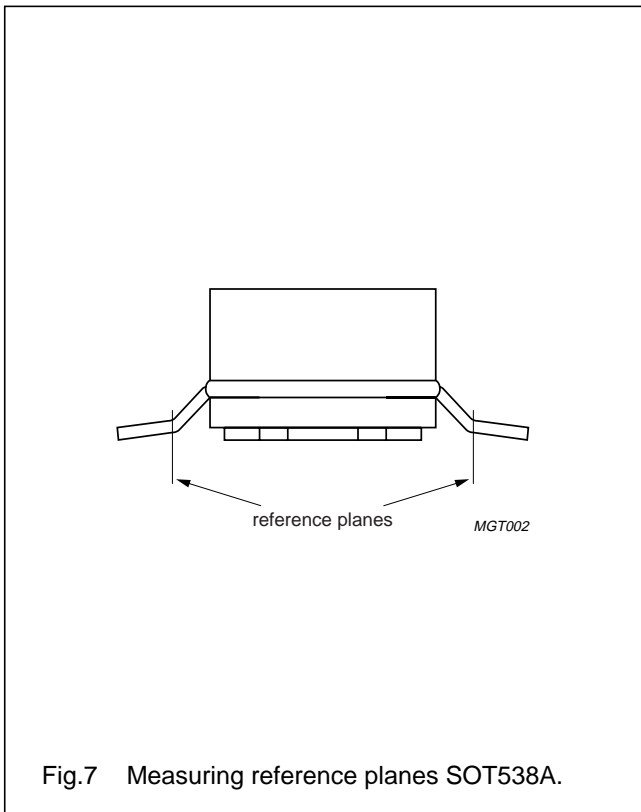
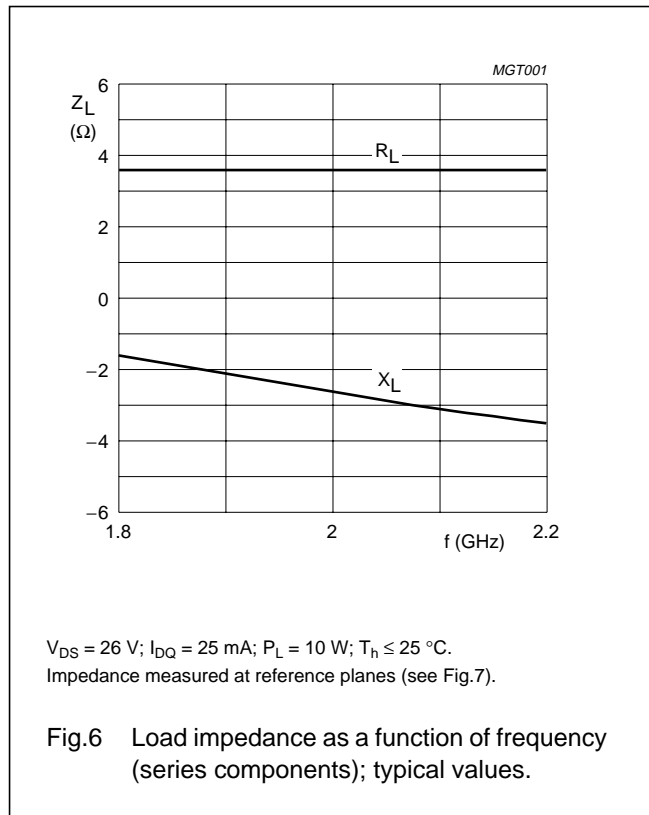
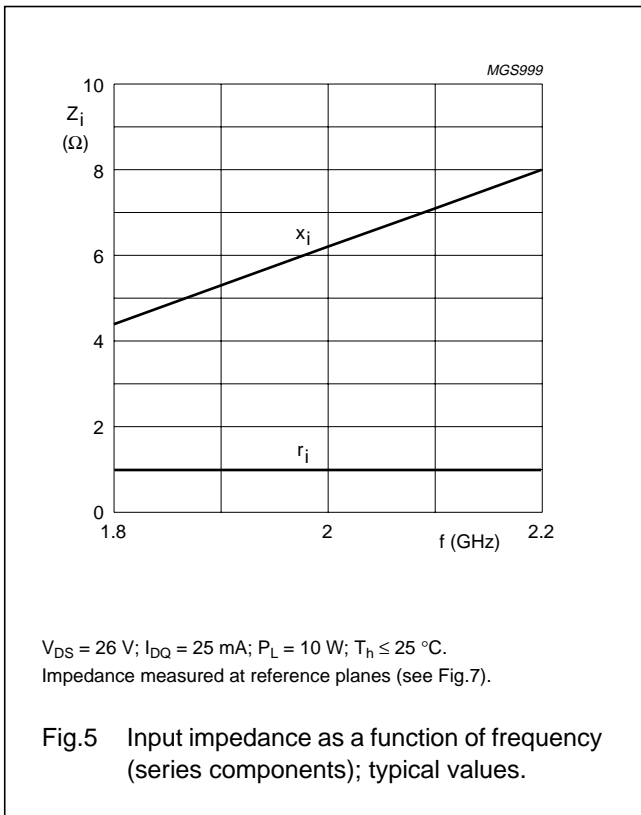


Fig.4 Third order intermodulation distortion as a function of peak envelope load power and  $I_{DQ}$  setting; typical values.

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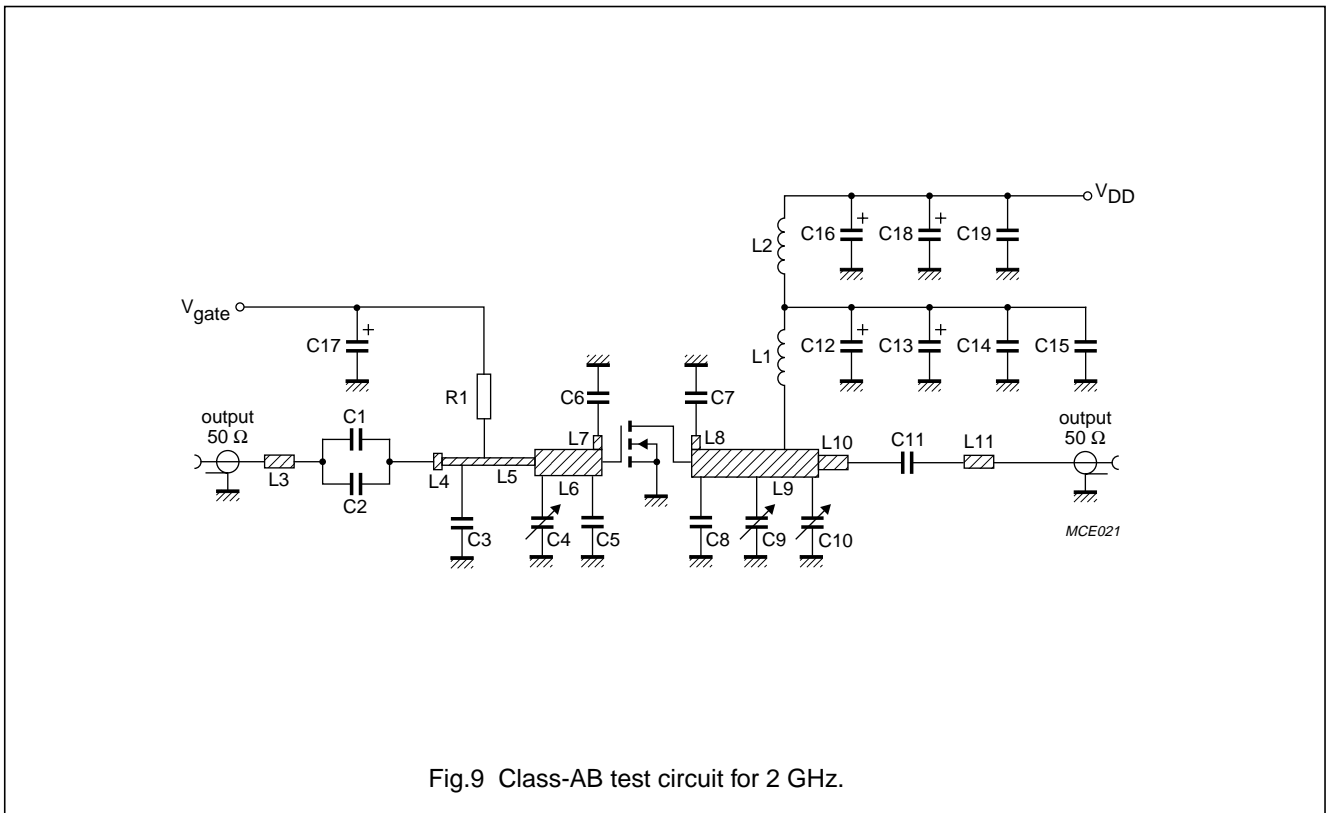


Fig.9 Class-AB test circuit for 2 GHz.

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## List of components (see Figs 8 and 9)

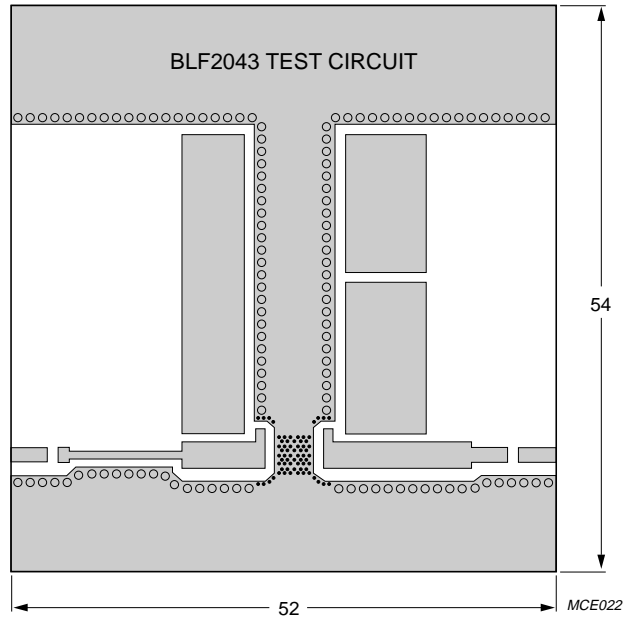
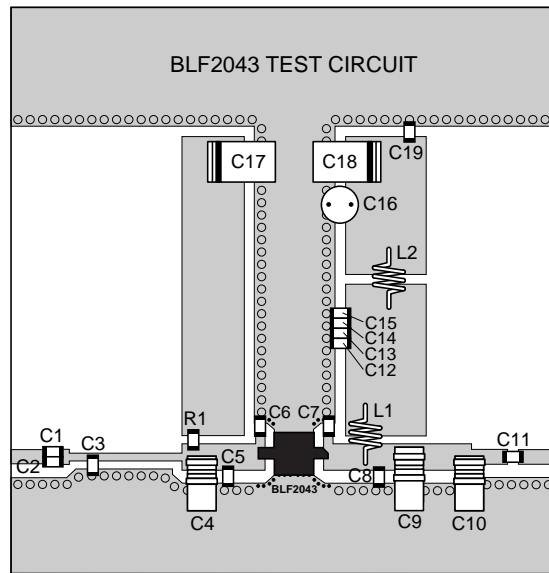
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	6.8 pF		
C3	multilayer ceramic chip capacitor; note 1	1.0 pF		
C4, C10, C11	tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C5, C7	multilayer ceramic chip capacitor; note 1	2.0 pF		
C6	multilayer ceramic chip capacitor; note 1	2.7 pF		
C8	multilayer ceramic chip capacitor; note 1	0.2 pF		
C9	multilayer ceramic chip capacitor; note 1	0.6 to 4.5 pF		
C12	multilayer ceramic chip capacitor; note 1	10 pF		
C13	multilayer ceramic chip capacitor; note 1	51 pF		
C14	multilayer ceramic chip capacitor; note 1	120 pF		
C15	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C16	electrolytic capacitor	100 $\mu$ F; 63 V		2222 037 58101
C17, C18	tantalum SMD capacitor	10 $\mu$ F; 35 V		
C19	multilayer ceramic chip capacitor; note 2	1 nF		
L1, L2	3 turns enamelled 0.5 mm copper wire		3 loops; d = 3 mm length = 3 mm	
L3	stripline; note 3	50 $\Omega$	3.5 $\times$ 1.5 mm	
L4	stripline; note 3	50 $\Omega$	1.0 $\times$ 1.5 mm	
L5	stripline; note 3	73.2 $\Omega$	5 $\times$ 2 mm	
L6	stripline; note 3	31 $\Omega$	11.0 $\times$ 0.8 mm	
L7, L8	stripline; note 3	64.7 $\Omega$	1.5 $\times$ 1.0 mm	
L9	stripline; note 3	31 $\Omega$	14.4 $\times$ 3.0 mm	
L10, L11	stripline; note 3	50 $\Omega$	3.5 $\times$ 1.5 mm	
R1	metal film resistor	2.2 k $\Omega$ ; 0.6 W		

## Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Rogers 5880 dielectric ( $\epsilon_r = 2.2$ ); thickness 0.51 mm.

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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ( $\epsilon_r = 2.2$ ), thickness 0.51 mm.

Fig.10 Component layout for 2 GHz class-AB test circuit.



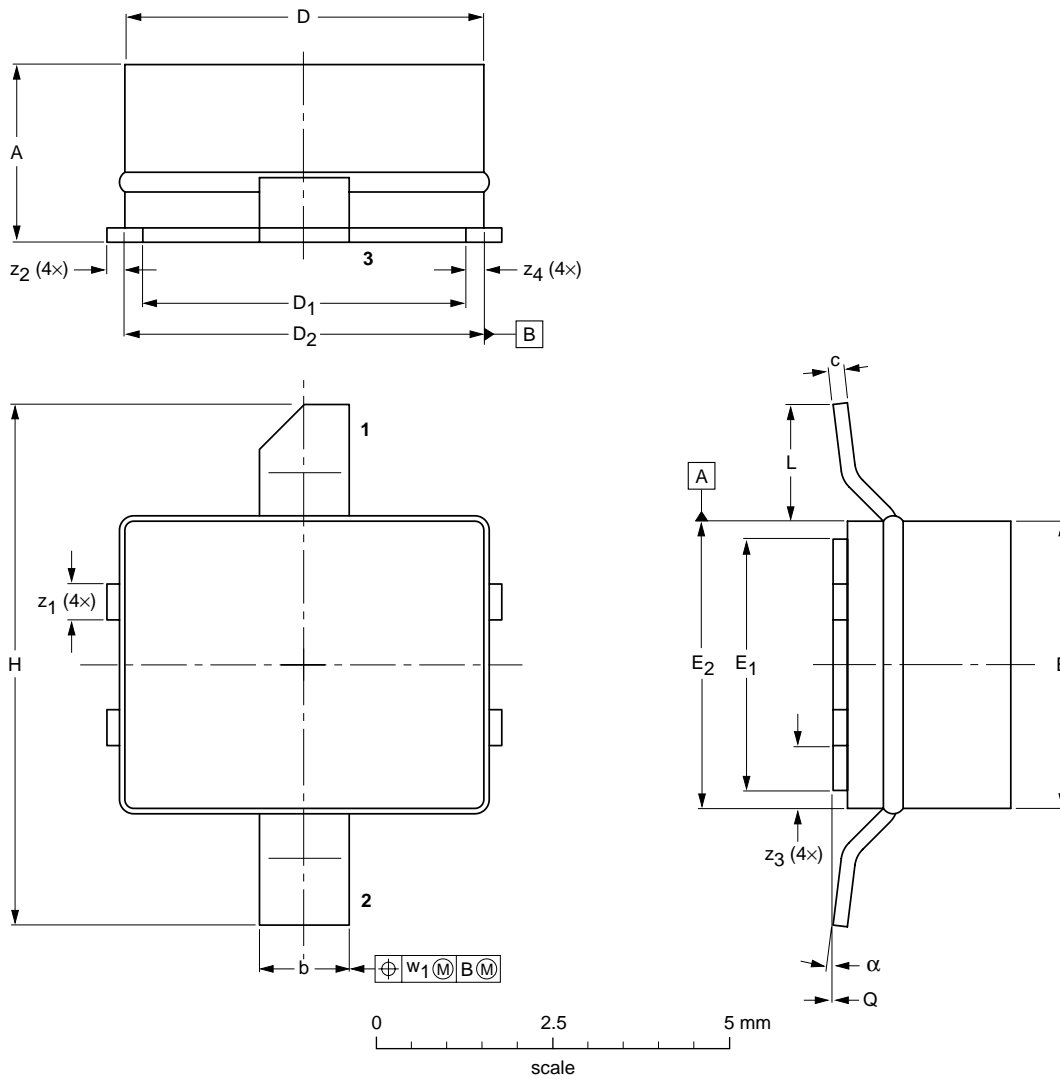
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PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads

SOT538A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	E <sub>2</sub>	H	L	Q	w <sub>1</sub>	z <sub>1</sub>	z <sub>2</sub>	z <sub>3</sub>	z <sub>4</sub>	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.16 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	0.58 0.43	0.25 0.18	0.97 0.81	0.51 0.00	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.203 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	0.023 0.017	0.010 0.007	0.038 0.032	0.020 0.000	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT538A						00-03-03- 02-08-20

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