HF/VHF power MOS transistor BLF221

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the HF/VHF frequency range.

This transistor is encapsulated in a 3-lead, SOT5 (TO-39/3) metal envelope, with the source connected to the case.

PINNING - TO-39/3

PIN	DESCRIPTION
1	drain
2	gate
3	source

PIN CONFIGURATION

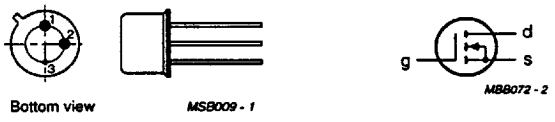

Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	2	> 10	> 50

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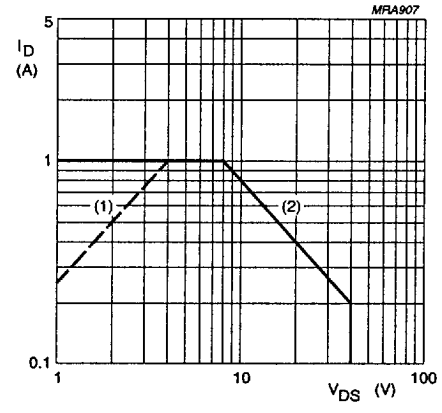
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	8	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

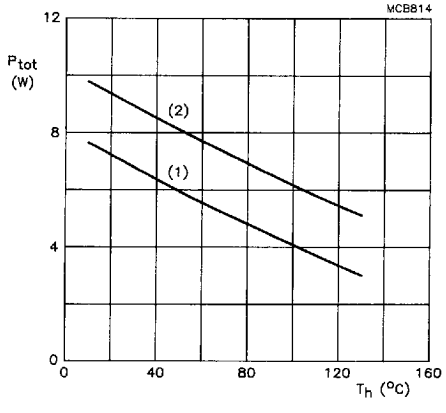
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	22 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

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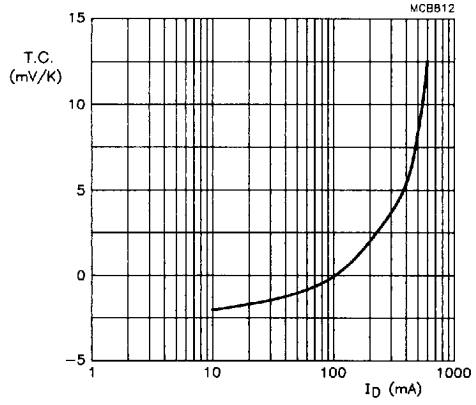
CHARACTERISTICS

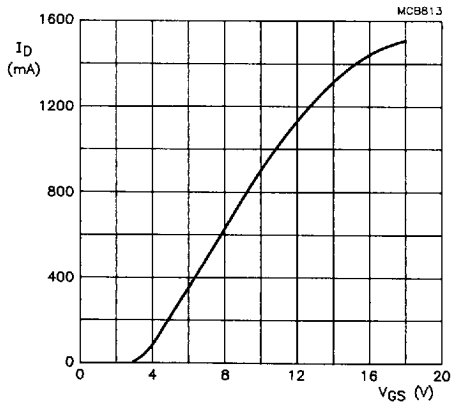
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 3 mA; V_{GS} = 0	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	10	μA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	80	135	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.5	4	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.3	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	5.3	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	7.8	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	1.8	–	pF



V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.

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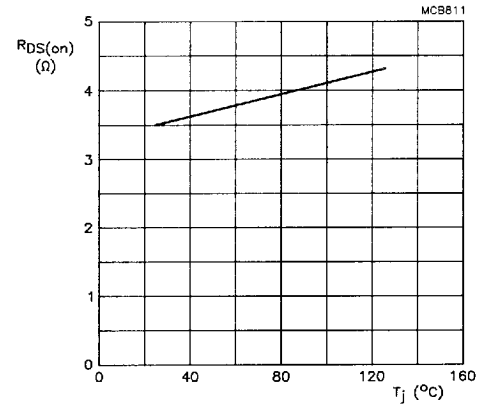
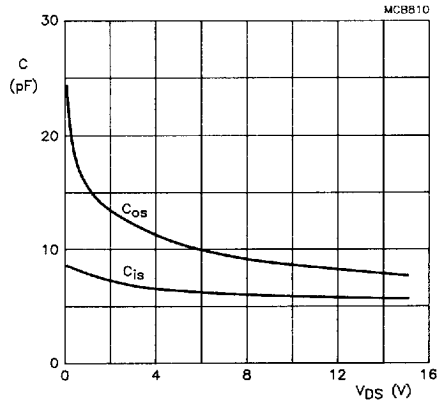


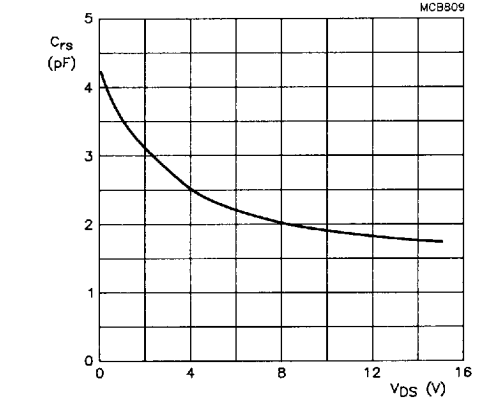
V_{GS} = 15 V; I_D = 0.3 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

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APPLICATION INFORMATION FOR CLASS-B OPERATION

T_{mb} = 25 °C; R_{GS} = 237 Ω; unless otherwise specified.

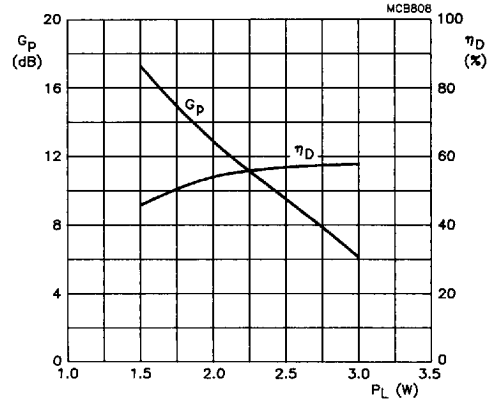
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	20	2	> 10 typ. 13	> 50 typ. 55

Ruggedness in class-B operation

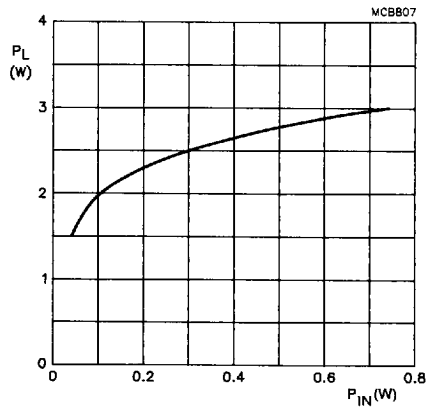
The BLF221 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 175 MHz at rated load power.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; f = 175 MHz.

Fig.9 Power gain and efficiency as a functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.

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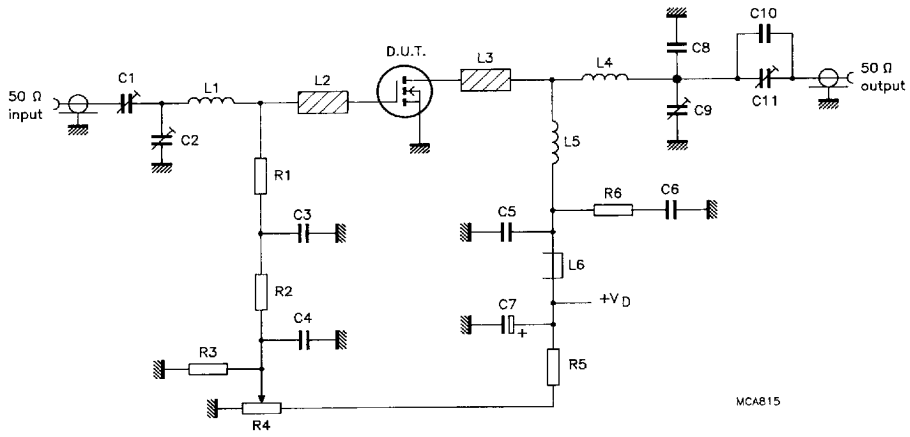

f = 175 MHz.

Fig.11 Test circuit for class-B operation.

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List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C11	film dielectric trimmer	2 to 9 pF		2222 809 09005
C2, C9	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3, C5	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C4, C6	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C7	Sprague electrolytic tantalum capacitor	2.2 µF, 35 V		
C8	multilayer ceramic chip capacitor (note 1)	5.1 pF, 500 V		
C10	multilayer ceramic chip capacitor (note 1)	9.1 pF, 500 V		
L1	6 turns enamelled 0.8 mm copper wire	137 nH	length 5.1 mm int. dia. 4.5 mm leads 2 x 5 mm	
L2, L3	stripline (note 2)	81 Ω	8 mm x 2 mm	
L4	3 turns enamelled 1 mm copper wire	57 nH	length 5 mm int. dia. 6 mm leads 2 x 5 mm	
L5	9 turns enamelled 1 mm copper wire	355 nH	length 11 mm int. dia. 7 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
R1	0.4 W metal film resistor	237 Ω		2322 151 72371
R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	10 turns cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 1.6 mm.

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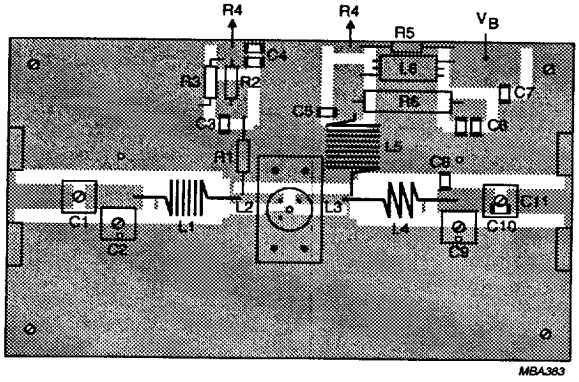

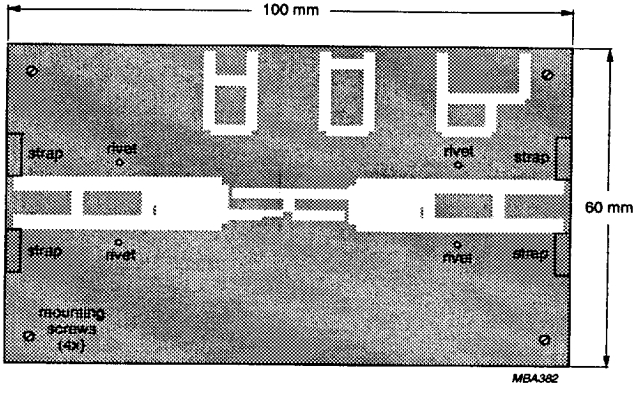

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets. Heatsinking is achieved by pressing the transistor against a brass thermal conductor (10 x 20 x 1.5 mm), which is connected to the heatsink by four screws.

Fig.12 Component layout for 175 MHz class-B test circuit.

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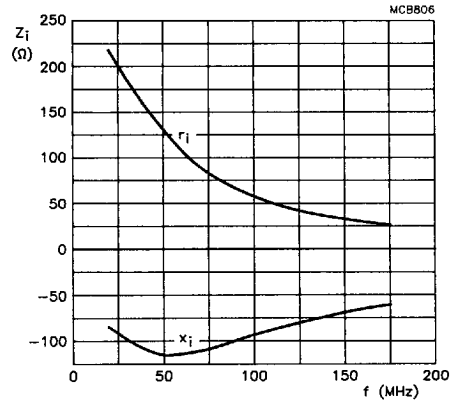
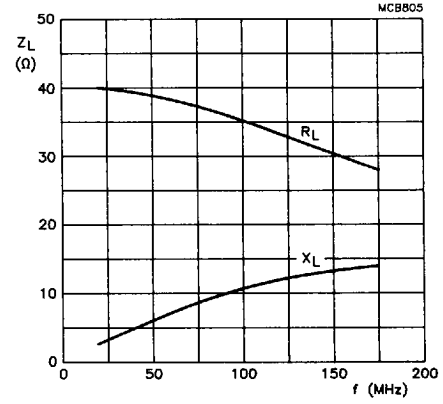


Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 237 Ω; P_L = 2 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 237 Ω; P_L = 2 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

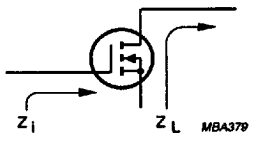
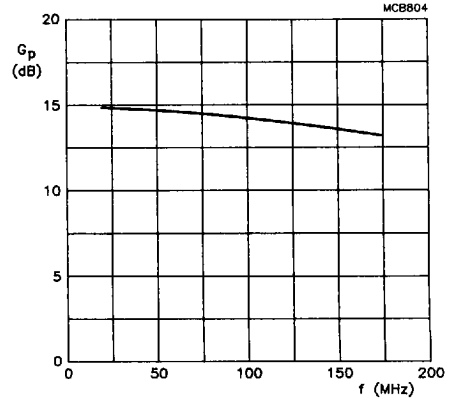


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 237 Ω; P_L = 2 W.

Fig.16 Power gain as a function of frequency, typical values.

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