VHF push-pull power MOS transistor

BLF246B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

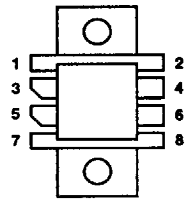
Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for large signal applications in the VHF frequency range.

The transistor is encapsulated in a balanced 8 lead, SOT161 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161

PIN	DESCRIPTION
1	source
2	source
3	drain 1
4	gate 1
5	drain 2
6	gate 2
7	source
8	source

PIN CONFIGURATION



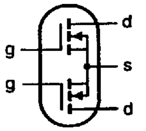


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	60	> 14	> 55

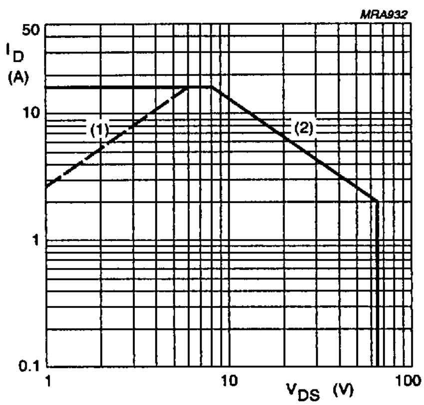
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	8	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	130	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

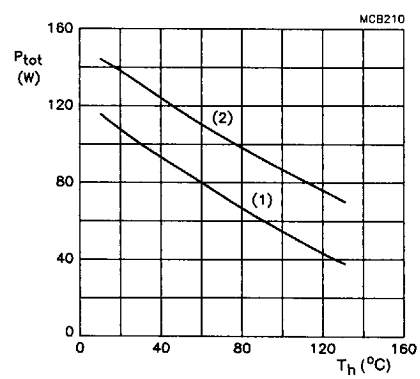
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



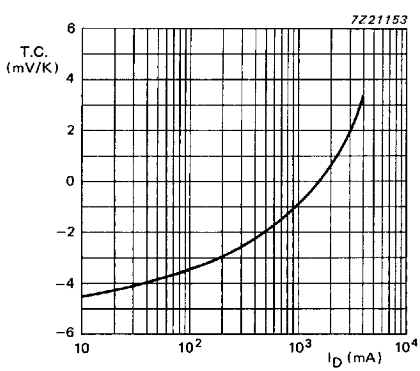
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

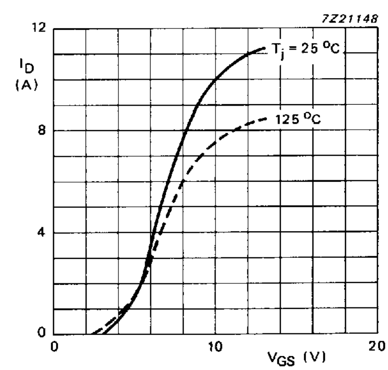
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	1.8	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	11	–	pF



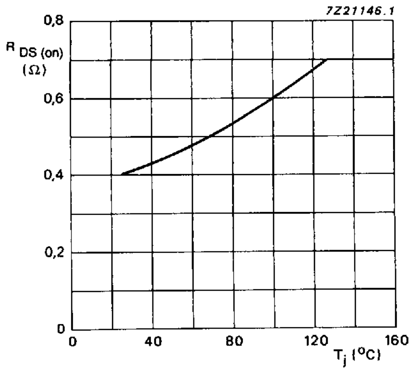
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



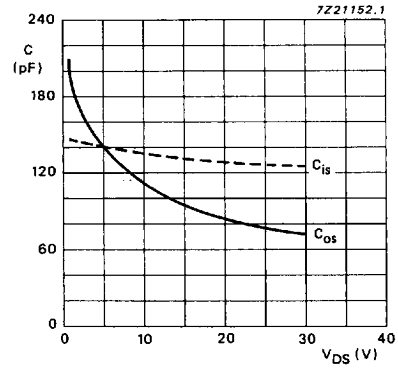
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



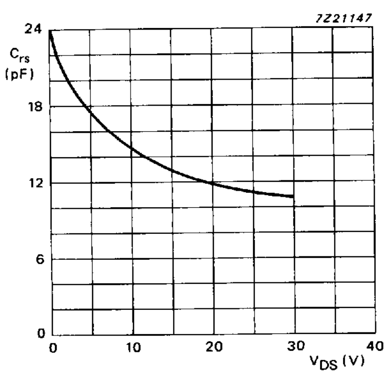
I_D = 1.5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

VHF push-pull power MOS transistor

BLF246B

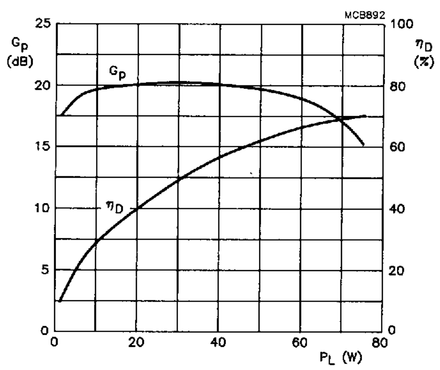
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.25 K/W; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2 x 50	60	> 14 typ. 19	> 55 typ. 65

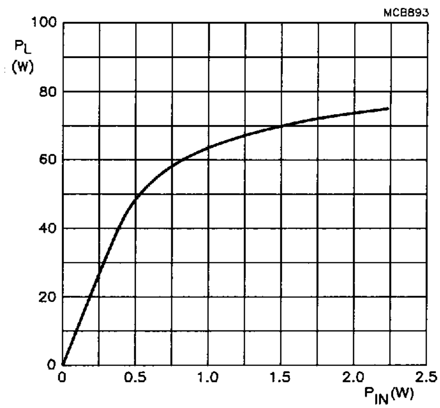
Ruggedness in class-B operation

The BLF246B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:
V_{DS} = 28 V, f = 175 MHz at rated output power.



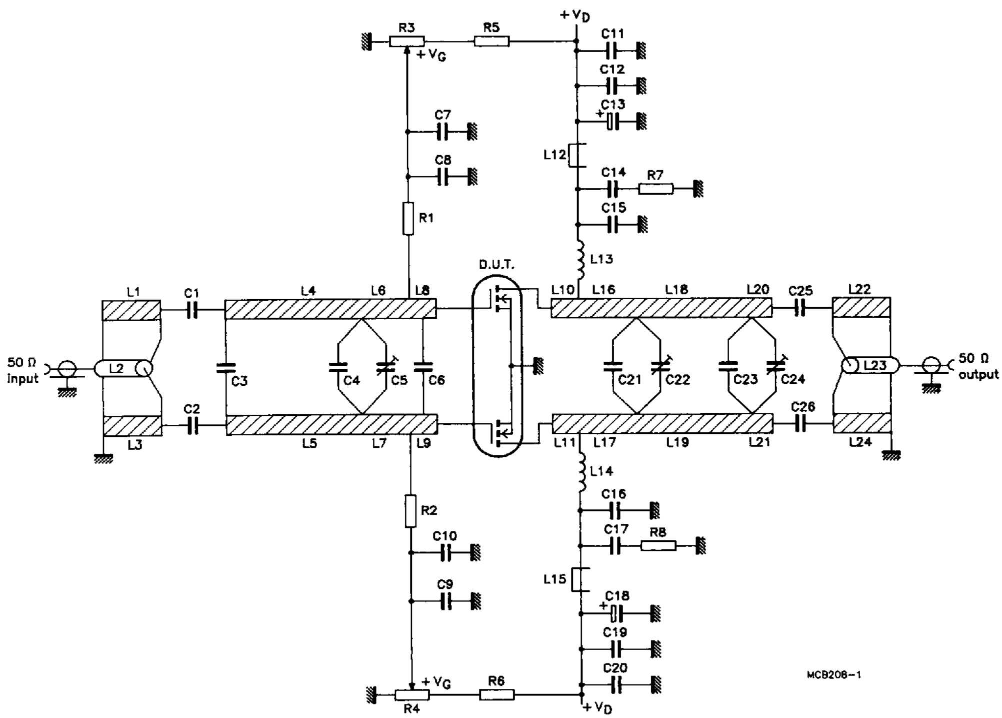
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.10 Load power as a function of drive power, typical values.



f = 175 MHz.

Fig.11 Test circuit for class-B operation.

List of components (class-B test circuit)

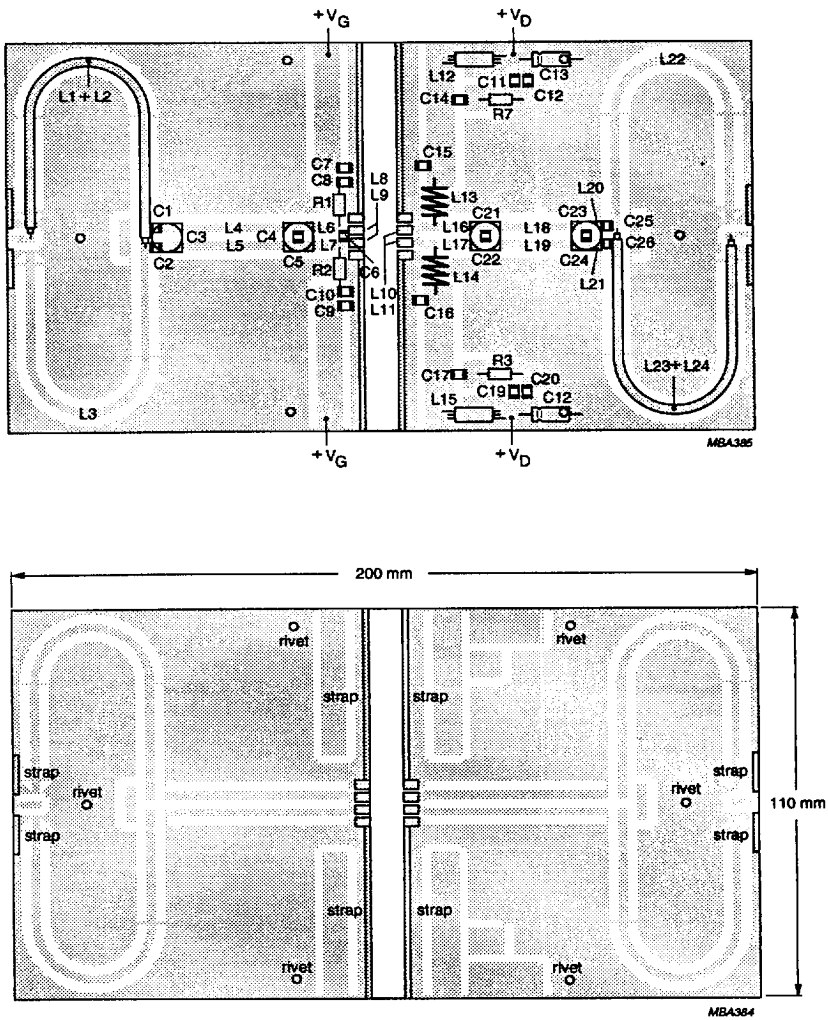
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C25, C26	multilayer ceramic chip capacitor (note 1)	91 pF		
C3	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4	multilayer ceramic chip capacitor (note 1)	180 pF		
C5, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6	multilayer ceramic chip capacitor (note 1)	100 pF		

VHF push-pull power MOS transistor

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8, C10, C15, C16	multilayer ceramic chip capacitor (note 1)	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 μF, 63 V		
C21	multilayer ceramic chip capacitor (note 1)	82 pF		
C23	multilayer ceramic chip capacitor (note 1)	33 pF		
L1, L3, L22, L24	stripline (note 2)	55 Ω	length 111 mm width 2.5 mm	
L2, L23	semi-rigid cable	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline (note 2)	50 Ω	length 6.5 mm width 2.8 mm	
L6, L7	stripline (note 2)	50 Ω	length 35 mm width 2.8 mm	
L8, L9	stripline (note 2)	50 Ω	length 5 mm width 2.8 mm	
L10, L11	stripline (note 2)	50 Ω	length 9 mm width 2.8 mm	
L12, L15	grade 3B Ferroxcube RF choke			4312 020 36642
L13, L14	4 turns enamelled 1 mm copper wire	50 nH	length 6.5 mm int. dia. 4 mm leads 2 x 5 mm	
L16, L17	stripline (note 2)	50 Ω	length 17 mm width 2.8 mm	
L18, L19	stripline (note 2)	50 Ω	length 26 mm width 2.8 mm	
L20, L21	stripline (note 2)	50 Ω	length 4 mm width 2.8 mm	
R1, R2, R7, R8	0.4 W metal film resistor	10 Ω		
R3, R4	10 turns potentiometer	50 kΩ		
R5, R6	0.4 W metal film resistor	205 kΩ		

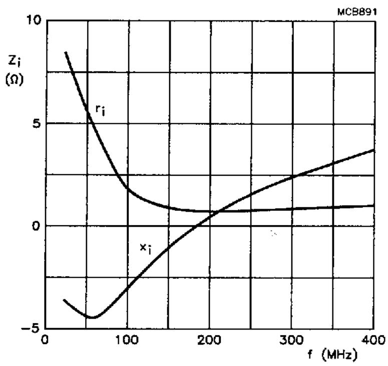
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric (ε_r = 4.5), thickness 1⁄16 inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.



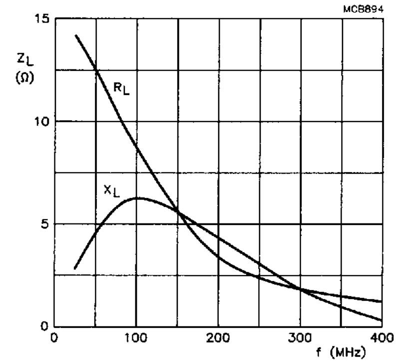
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

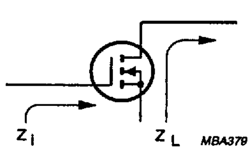
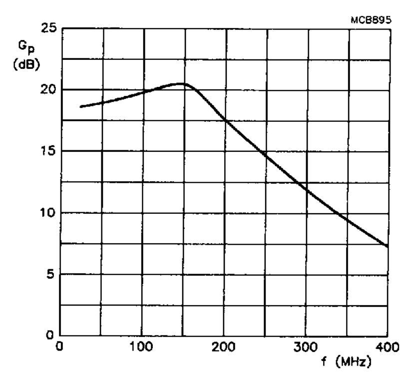


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.