UHF push-pull power MOS transistor

BLF544B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT268

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION

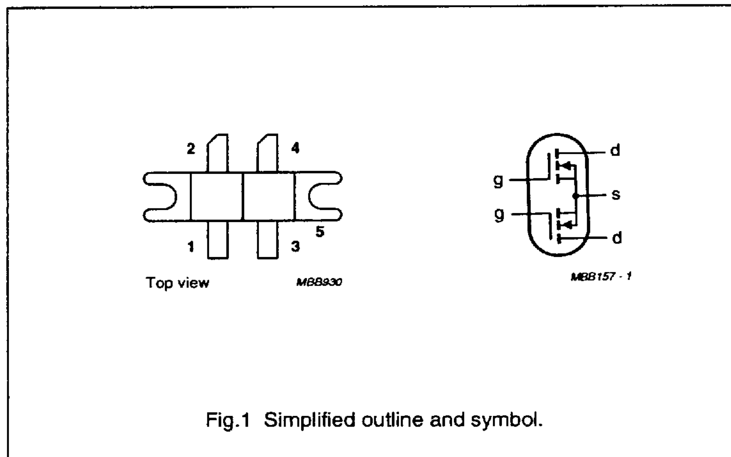

Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	20	> 12	> 50

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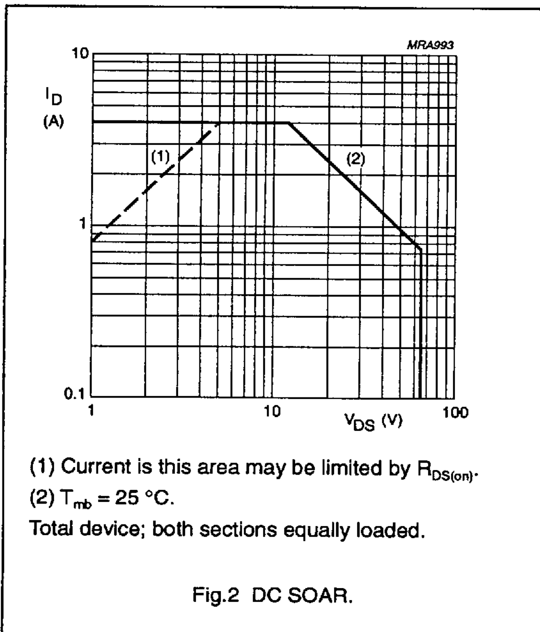
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	2	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	48	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

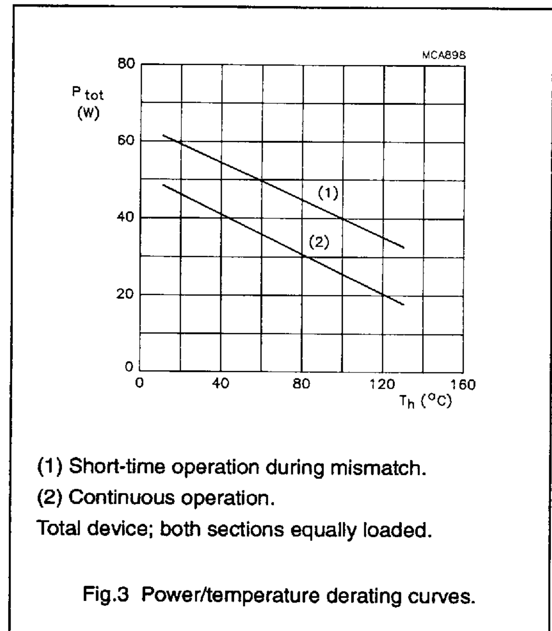
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	3.7 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.
(2) Continuous operation.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

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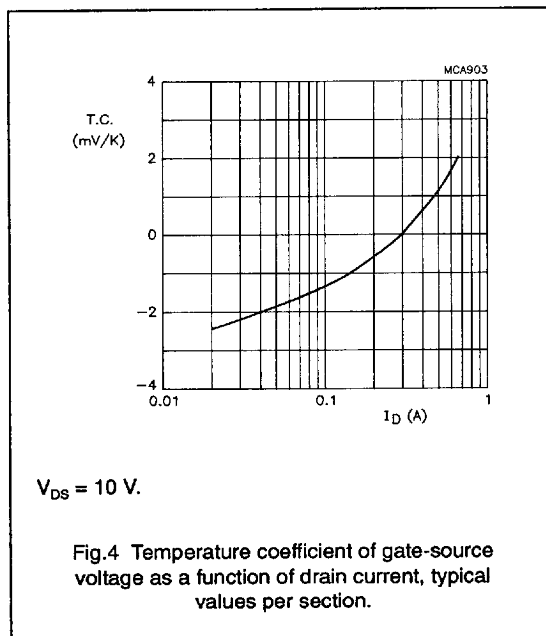
CHARACTERISTICS (per section)

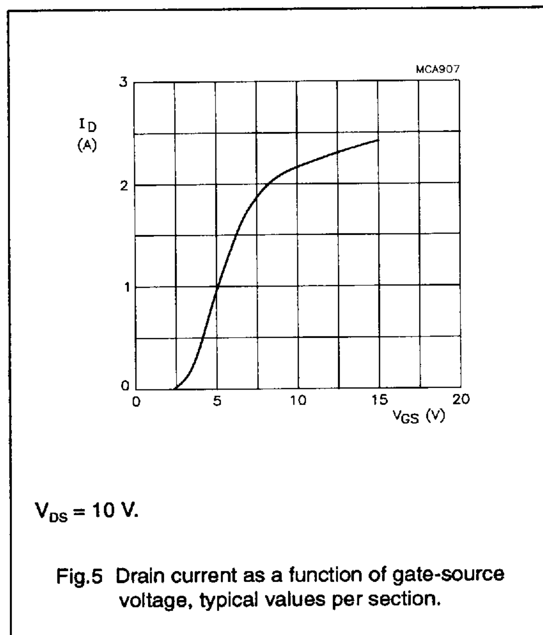
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 5 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 20 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 0.6 A; V_{DS} = 10 V	300	450	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.6 A; V_{GS} = 10 V	–	0.7	2.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.4	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	16	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	12	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	3.2	–	pF



V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.

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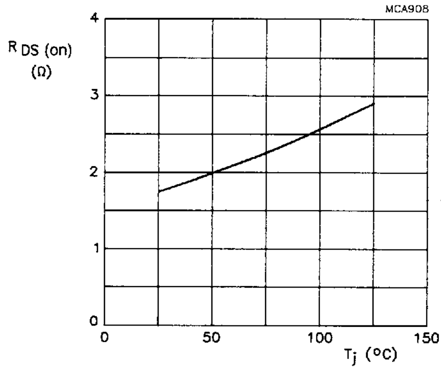
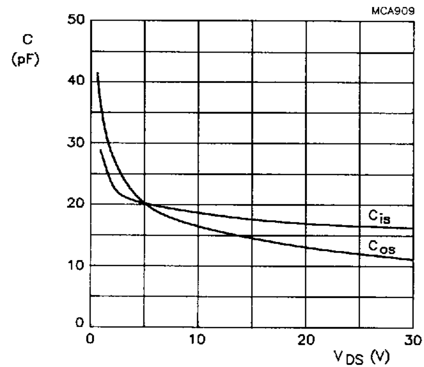


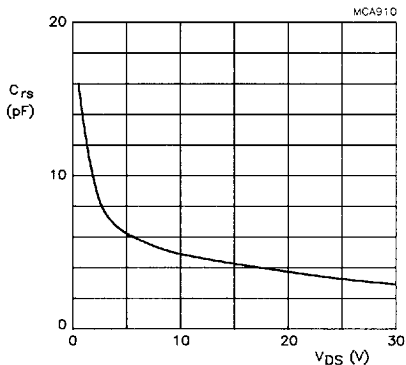
I_D = 0.6 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

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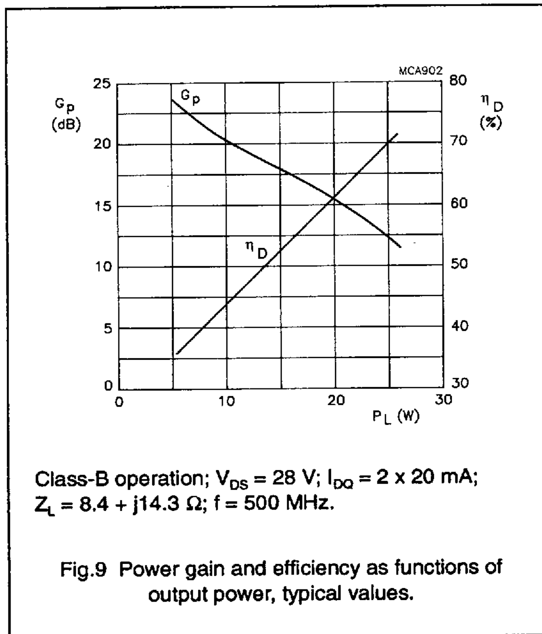
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 20	20	> 12 typ. 15	> 50 typ. 60

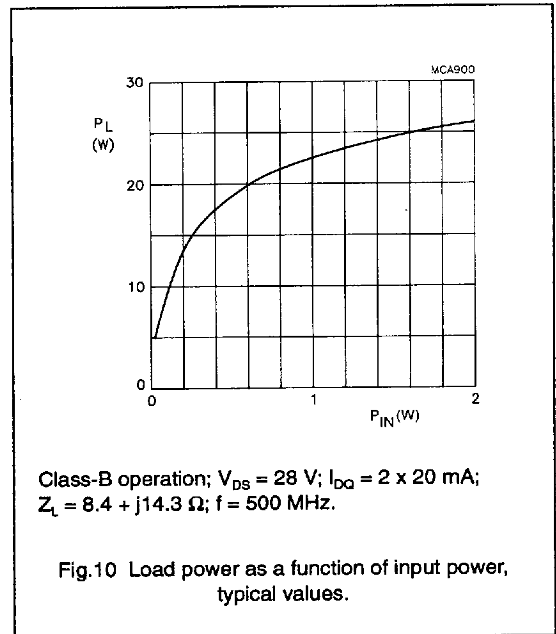
Ruggedness in class-B operation

The BLF544B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:
V_{DS} = 28 V, f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.

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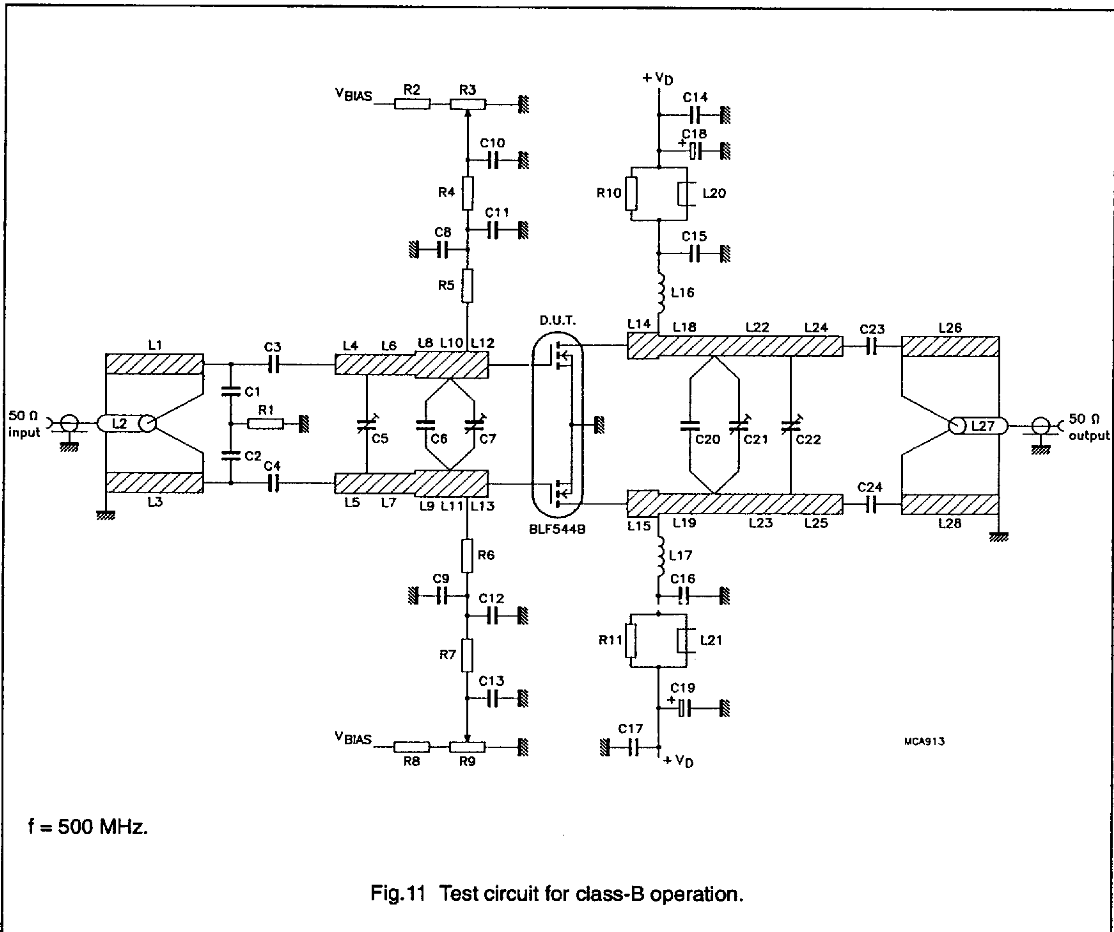

Fig.11 Test circuit for class-B operation.

List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	9.1 pF, 500 V		
C3, C4, C6	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C5	film dielectric trimmer	2 to 9 pF		2222 809 09005
C7, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C8, C9, C15, C16	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		

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COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C10, C13	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C11, C12, C14, C17	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C18, C19	electrolytic capacitor	10 µF, 63 V		2222 030 38109
C20	multilayer ceramic chip capacitor (note 1)	6.8 pF, 500 V		
C23, C24	multilayer ceramic chip capacitor (note 1)	16 pF, 500 V		
L1, L3, L26, L28	stripline (note 2)	50 Ω	56 x 2.4 mm	
L2	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
L4, L5	stripline (note 2)	56 Ω	8 x 2 mm	
L6, L7	stripline (note 2)	56 Ω	15.5 x 2 mm	
L8, L9	stripline (note 2)	42 Ω	10 x 3 mm	
L10, L11	stripline (note 2)	42 Ω	5 x 3 mm	
L12, L13, L14, L15	stripline (note 2)	42 Ω	6 x 3 mm	
L16, L17	6 turns enamelled 1 mm copper wire	124 nH	length 8.5 mm int. dia. 5.4 mm leads 2 x 5 mm	
L18, L19	stripline (note 2)	56 Ω	22 x 2 mm	
L20, L21	grade 3B Ferroxcube RF choke			4312 020 36642
L22, L23	stripline (note 2)	56 Ω	18 x 2 mm	
L24, L25	stripline (note 2)	56 Ω	16 x 2 mm	
L27	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
R1	0.4 W metal film resistor	5.62 Ω		2322 151 75628
R2, R8	0.4 W metal film resistor	11.5 kΩ		2322 151 71159
R3, R9	10 turns potentiometer	5 kΩ		
R4, R7	0.4 W metal film resistor	590 Ω		2322 151 75901
R5, R6	0.4 W metal film resistor	46.4 Ω		2322 151 74649
R10, R11	1 W metal film resistor	10 Ω		2322 153 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric (ε_r =2.2), thickness 1/32 inch.
3. Semi-rigid cables L2 and L27 are soldered on to striplines L1 and L26.

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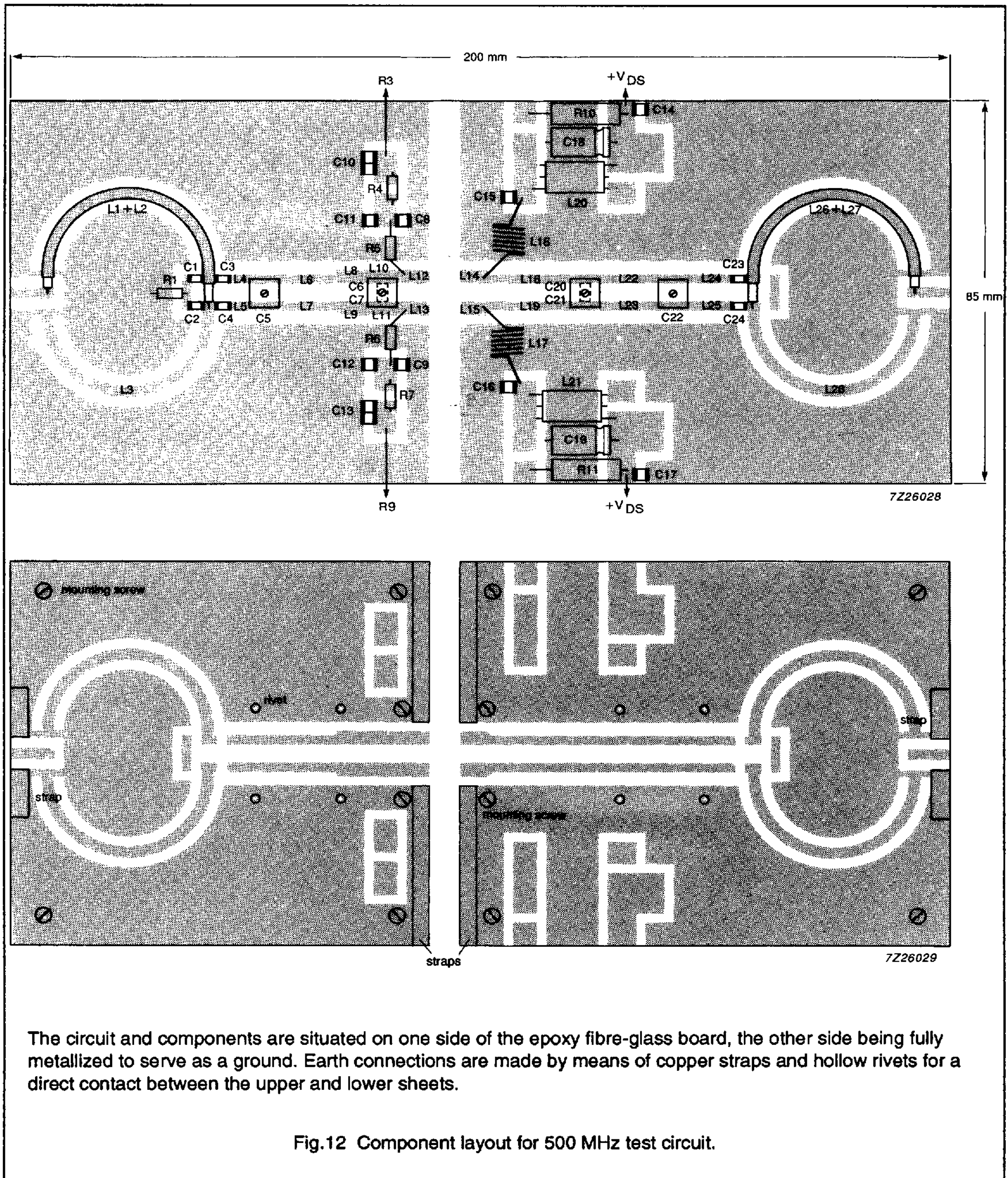

The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.

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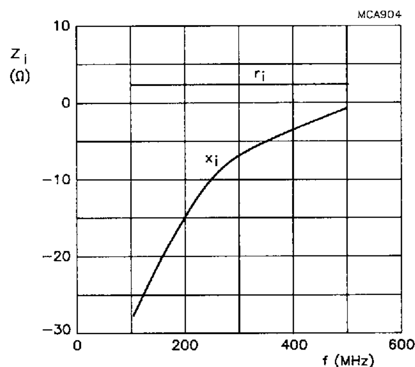
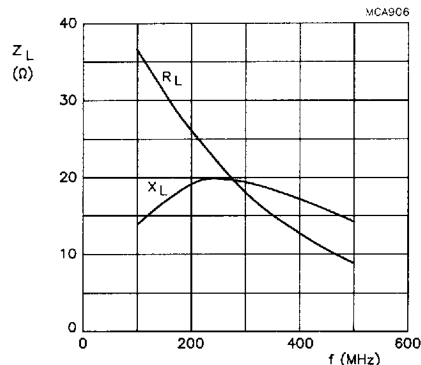


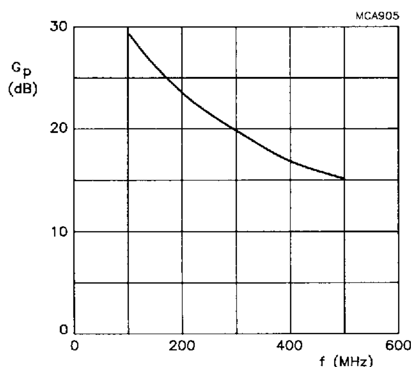
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; P_L = 20 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; P_L = 20 W.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; P_L = 20 W.

Fig.15 Power gain as a function of frequency, typical values per section.

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