

# BLF6G15L-40RN; BLF6G15LS-40RN

Power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

40 W LDMOS power transistor for base station applications at frequencies from 1450 MHz to 1550 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a class-AB production test circuit.

Test signal	f (MHz)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR (dBc)
2-carrier W-CDMA	1476 to 1511	28	2.5	22.5	13.5	-45 <sup>[1]</sup>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at probability of 0.01 % on CCDF carrier; carrier spacing 5 MHz.

### 1.2 Features and benefits

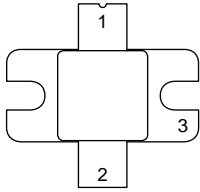
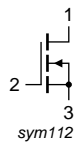
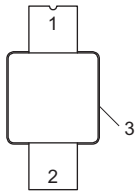
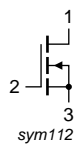
- Typical 2-carrier W-CDMA performance at frequencies of 1476 MHz and 1511 MHz, a supply voltage of 28 V and an  $I_{DQ}$  of 375 mA:
  - ◆ Average output power = 2.5 W
  - ◆ Power gain = 22.5 dB
  - ◆ Efficiency = 13.5 %
  - ◆ ACPR = -45 dBc
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1450 MHz to 1550 MHz)
- Internally matched for ease of use
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC.

### 1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 1450 MHz to 1550 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF6G15L-40RN (SOT1135A)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		
<b>BLF6G15LS-40RN (SOT1135B)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G15L-40RN	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT1135A
BLF6G15LS-40RN	-	earless flanged ceramic package; 2 leads	SOT1135B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 2.5\text{ W (CW)}$	1.30	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ °C}$  per section; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.59\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 59\text{ mA}$	1.4	1.8	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	9.4	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 58.9\text{ mA}$	-	0.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 2.06\text{ A}$	-	0.32	-	$\Omega$

## 7. Application information

**Table 7. 2-carrier W-CDMA RF performance**

Class-AB production test circuit; PAR 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz; 3GPP test model 1; 64 DPCH;  $f_1 = 1476\text{ MHz}; f_2 = 1511\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 375\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	2.5	-	W
$G_p$	power gain	$P_{L(AV)} = 2.5\text{ W}$	19.8	22.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 2.5\text{ W}$	-	-16	-11	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 2.5\text{ W}$	11.5	13.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 2.5\text{ W}$	-	-45	-40	dBc

### 7.1 Ruggedness in Class-AB operations

The BLF6G15L-40RN and the BLF6G15LS-40RN are capable of withstanding a load mismatch corresponding to VSWR 10 : 1 through all phases under following conditions:  $V_{DS} = 28\text{ V}; I_{Dq} = 375\text{ mA}; P_L = 40\text{ W}; f = 1476\text{ MHz}$  (CW).

## 8. Test information

### 8.1 Impedance information

**Table 8. Typical impedance**

Measured load-pull data. Typical values per section.  $I_{Dq} = 330\text{ mA}$ ; main transistor  $V_{DS} = 28\text{ V}$   $Z_S$  and  $Z_L$  defined in [Figure 1](#).

f (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
1450	4.4 – j5.9	5.5 – j4.6
1480	4.4 – j4.1	5.0 – j5.0
1510	6.4 – j4.7	5.0 – j5.0

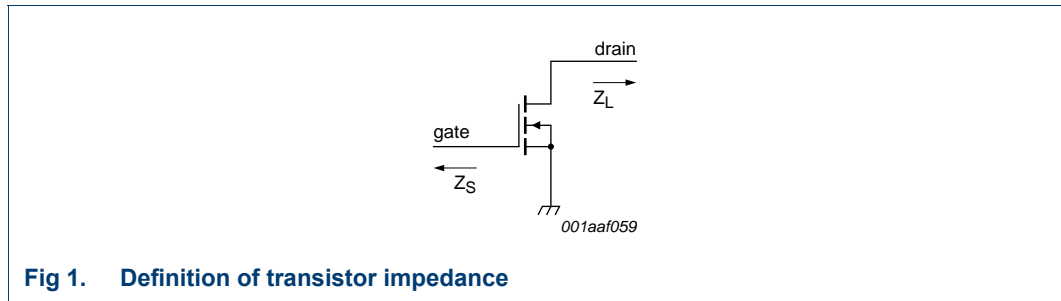


Fig 1. Definition of transistor impedance

## 8.2 One-tone graphs

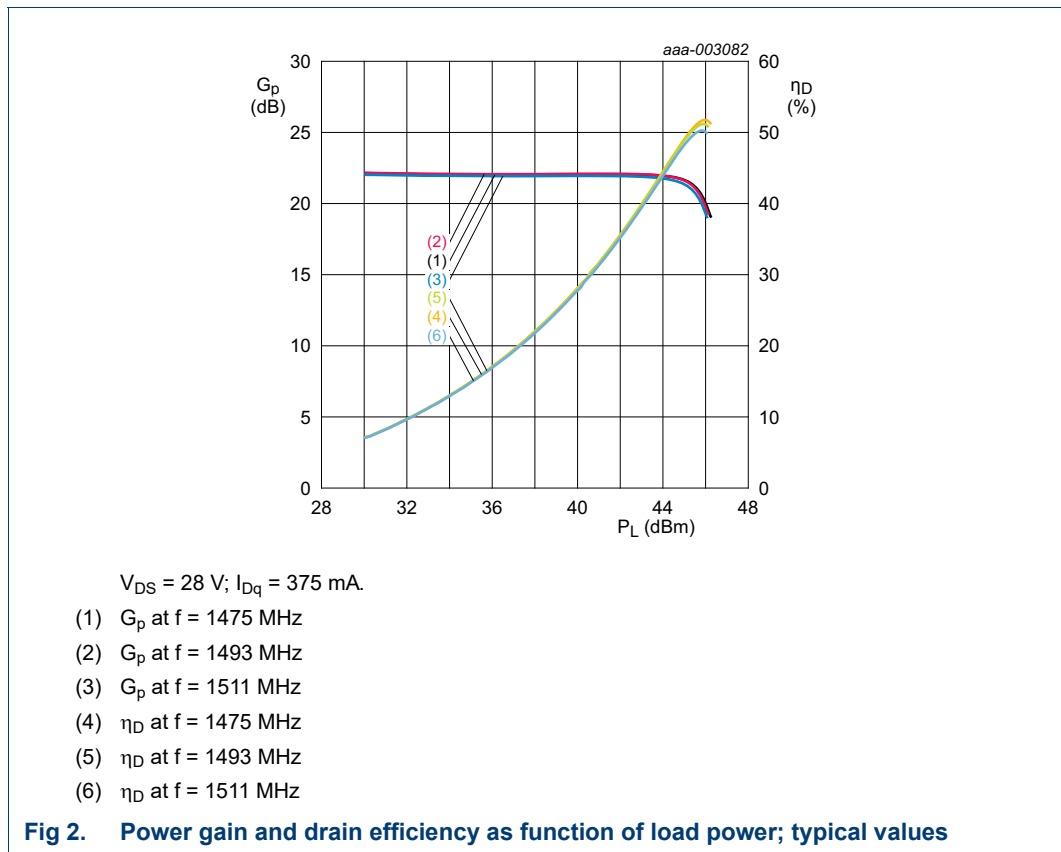
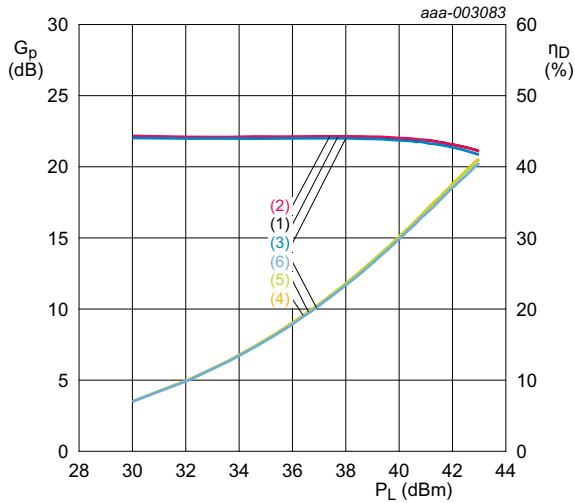


Fig 2. Power gain and drain efficiency as function of load power; typical values

8.3 2-Carrier W-CDMA graphs

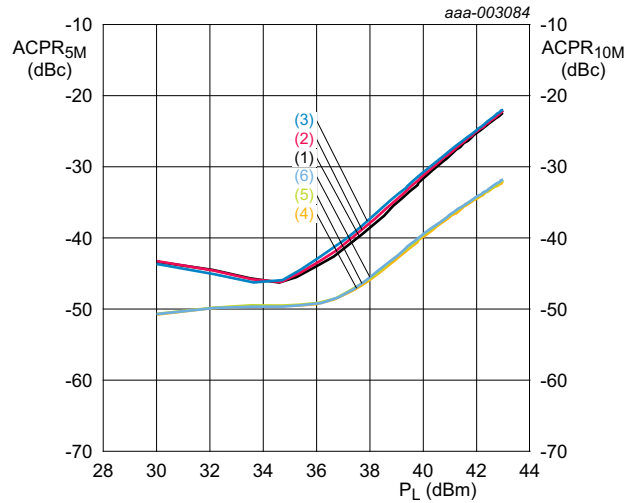
3GPP, test model 1; 64 DPCH, PAR = 8.4 dB at 0.01 % probability, 5 MHz carrier spacing.



$T_{amb} = 25\text{ }^\circ\text{C}$ .

- (1)  $G_p$  at  $f = 1475\text{ MHz}$
- (2)  $G_p$  at  $f = 1493\text{ MHz}$
- (3)  $G_p$  at  $f = 1511\text{ MHz}$
- (4)  $\eta_D$  at  $f = 1475\text{ MHz}$
- (5)  $\eta_D$  at  $f = 1493\text{ MHz}$
- (6)  $\eta_D$  at  $f = 1511\text{ MHz}$

Fig 3. Power gain and drain efficiency as function of load power; typical values

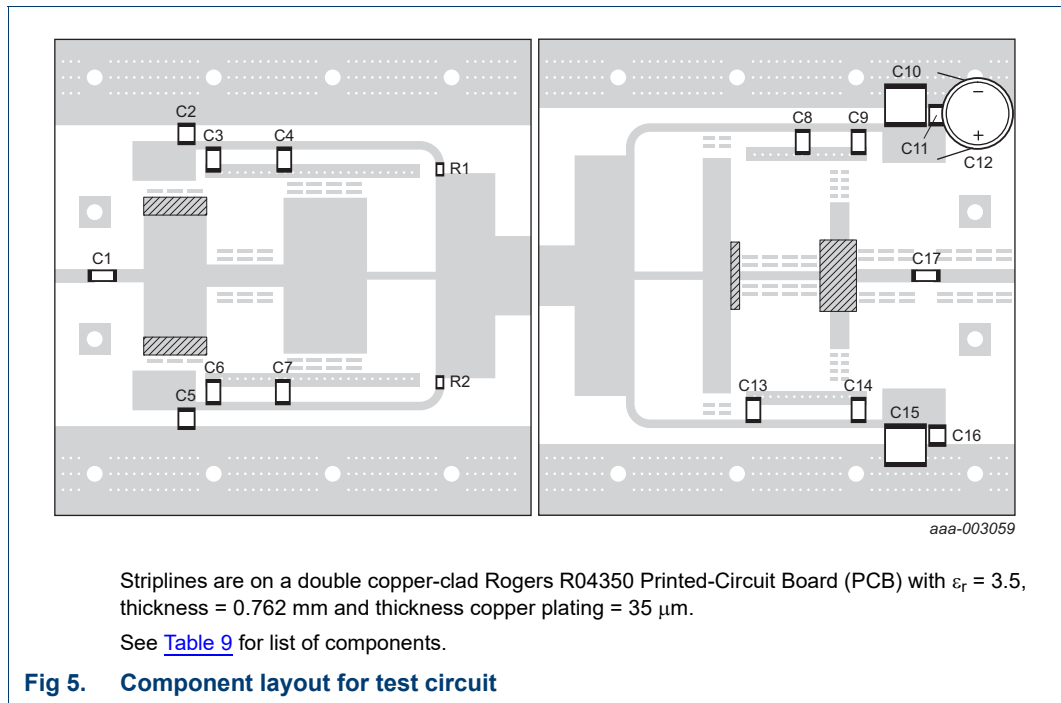


$T_{amb} = 25\text{ }^\circ\text{C}$ .

- (1)  $ACPR_{5M}$  at  $f = 1475\text{ MHz}$
- (2)  $ACPR_{5M}$  at  $f = 1493\text{ MHz}$
- (3)  $ACPR_{5M}$  at  $f = 1511\text{ MHz}$
- (4)  $ACPR_{10M}$  at  $f = 1475\text{ MHz}$
- (5)  $ACPR_{10M}$  at  $f = 1493\text{ MHz}$
- (6)  $ACPR_{10M}$  at  $f = 1511\text{ MHz}$

Fig 4. Adjacent channel power ratio (5 MHz and 10 MHz) as a function of load power; typical values

8.4 Test circuit



**Table 9. List of components**

For test circuit, see [Figure 5](#).

Component	Description	Value	Remarks
C1, C17	multilayer ceramic chip capacitor	24 pF	[1]
C3, C6	multilayer ceramic chip capacitor	68 pF	[2]
C4, C7, C8	multilayer ceramic chip capacitor	150 pF	[2]
C9, C14	multilayer ceramic chip capacitor	47 pF	[2]
C13	multilayer ceramic chip capacitor	15 pF	[2]
C2, C5, C11, C16	multilayer ceramic chip capacitor	10 $\mu\text{F}$	[3]
C10, C15	multilayer ceramic chip capacitor	0.1 $\mu\text{F}$	[3]
C12	electrolytic capacitor	2200 $\mu\text{F}$ , 50 V	
R1, R2	chip resistor	15 $\Omega$	

[1] American technical ceramics type 800B or capacitor of same quality.

[2] American technical ceramics type 100B or capacitor of same quality.

[3] TDK or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT1135A

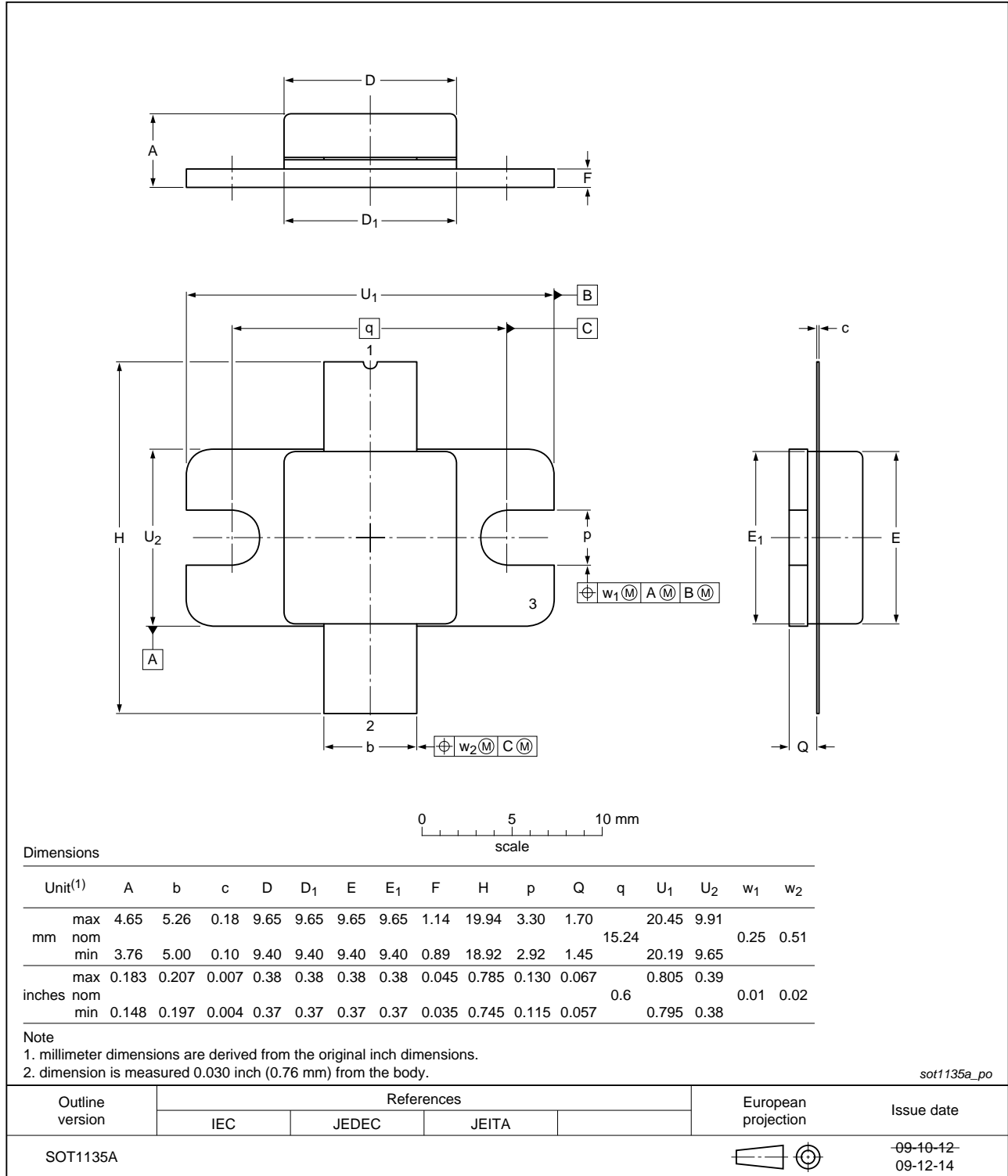
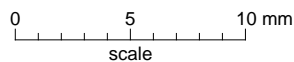
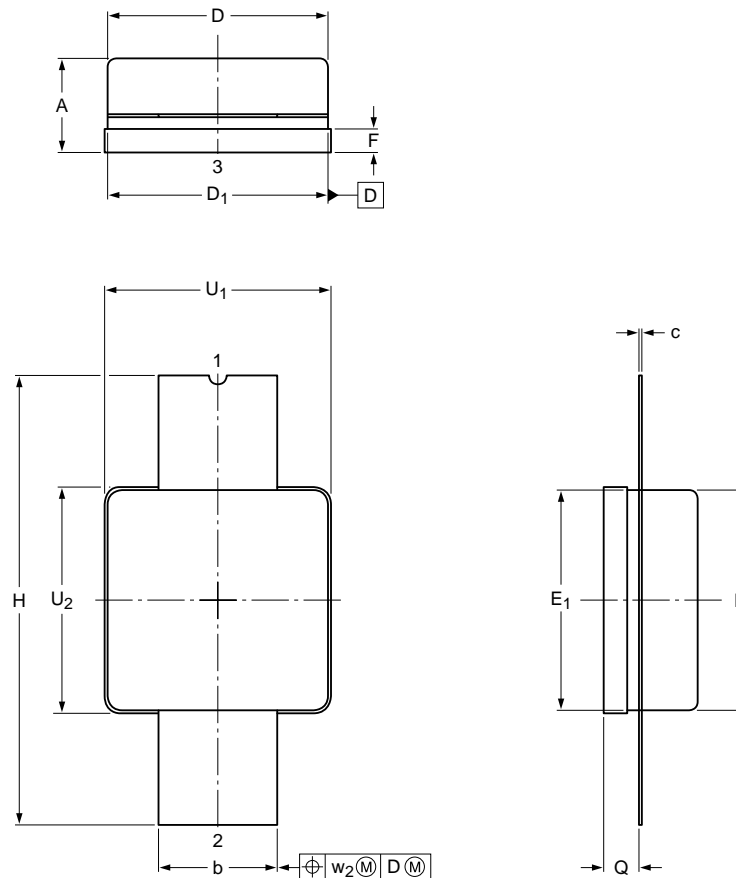


Fig 6. Package outline SOT1135A

Earless flanged ceramic package; 2 leads

SOT1135B



Dimensions

Unit <sup>(1)</sup>	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	Q	U <sub>1</sub>	U <sub>2</sub>	w <sub>2</sub>
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	1.14	19.94	1.70	9.91	9.91	0.51
	nom												
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	1.45	9.65	
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.045	0.785	0.067	0.39	0.39	0.02
	nom												
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.057	0.38	

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135b\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1135B					-09-10-12- 09-12-14

Fig 7. Package outline SOT1135B



## 10. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 11. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average Ratio
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 12. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G15L-40RN_6G15LS-40RN#3	20150901	Product data sheet	-	BLF6G15L-40RN_6G15LS-40RN v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLF6G15L-40RN_6G15LS-40RN v.2	20120514	Product data sheet	-	BLF6G15L-40RN_6G15LS-40RN v.1
BLF6G15L-40RN_6G15LS-40RN v.1	20111027	Objective data sheet	-	-

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### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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