BLF7G10L-250; BLF7G10LS-250

Power LDMOS transistor

Rev. 3 — 16 February 2012 Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor for base station applications at frequencies from 920 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	920 to 960	1800	30	60	19.5	30.5	−34 [1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier. Carrier spacing 5 MHz.

1.2 Features and benefits

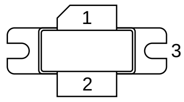
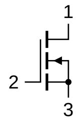
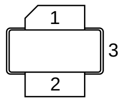
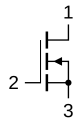
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (920 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use (input and output)
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 920 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF7G10L-250 (SOT502A)				
1	drain			 sym112
2	gate			
3	source	[1]		
BLF7G10LS-250 (SOT502B)				
1	drain			 sym112
2	gate			
3	source	[1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G10L-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF7G10LS-250	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 60 W (CW); V_{DS} = 30 V; I_{Dq} = 1800 mA	0.38	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 330 mA	1.50	1.9	2.30	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	56	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	0.5	mA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11.55 A	-	22	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 11.55 A	-	57	-	mΩ

7. Test information

Table 7. Functional test information

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 920 MHz; f_2 = 925 MHz; f_3 = 955 MHz; f_4 = 960 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 1800 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 60 W	18.5	19.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 60 W	-	−15.5	−10	dB
η_D	drain efficiency	$P_{L(AV)}$ = 60 W	27	30.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 60 W	-	−34	−31	dBc

7.1 Ruggedness in class-AB operation

The BLF7G10L-250 and BLF7G10LS-250 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 1800 mA; P_L = 200 W (CW); f = 920 MHz to 960 MHz.

7.2 Impedance information

Table 8. Typical impedance information
I_{Dq} = 1800 mA; main transistor V_{DS} = 30 V.
Z_S and Z_L defined in Figure 1.

f (MHz)	Z_S (Ω)	Z_L (Ω)
925	3.1 – j3.3	1.0 – j1.7
942	3.2 – j3.3	1.0 – j1.6
960	3.4 – j3.5	0.9 – j1.4

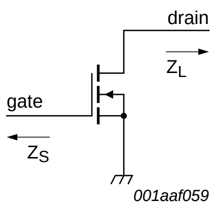
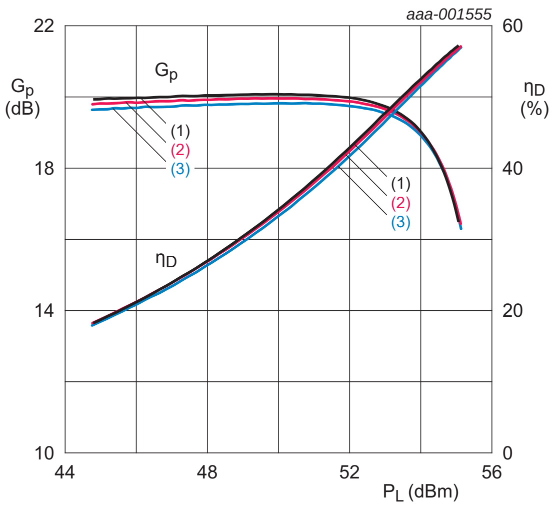


Fig 1. Definition of transistor impedance

7.3 CW pulsed



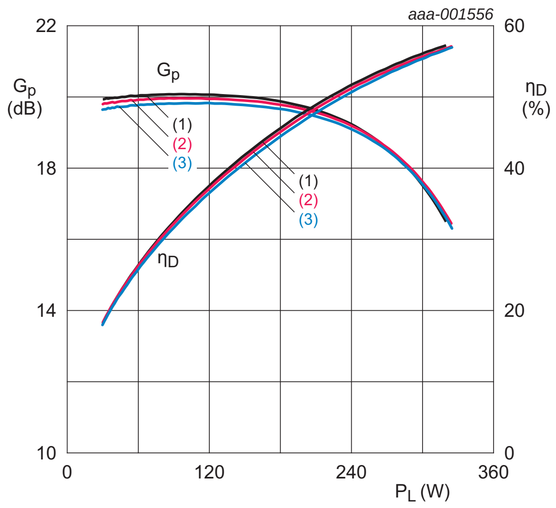
V_{DS} = 30 V; I_{Dq} = 1800 mA.

(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 2. Power gain and drain efficiency as function of output power; typical values



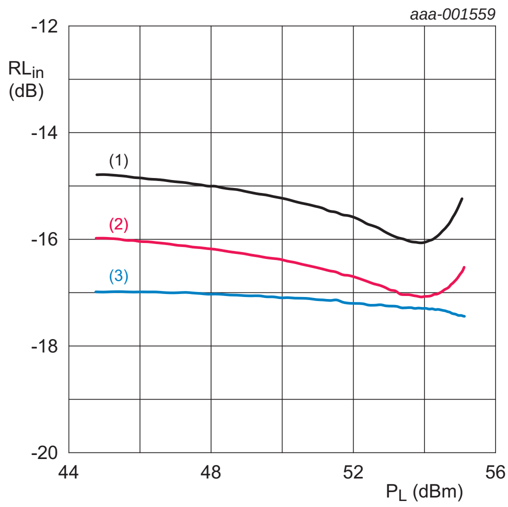
V_{DS} = 30 V; I_{Dq} = 1800 mA.

(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 1800 mA.

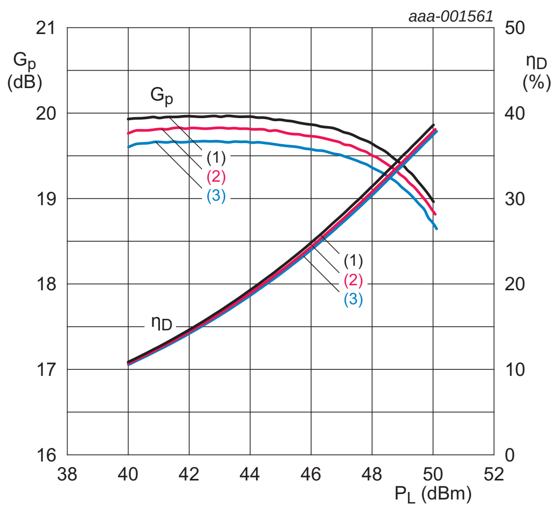
(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 4. Input return loss as a function of output power; typical values

7.4 2C-WCDMA



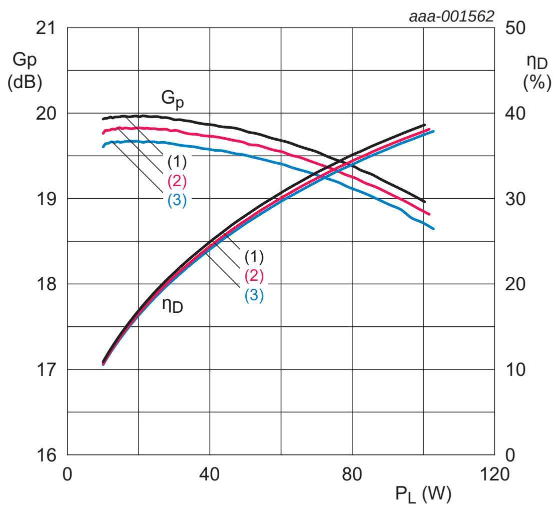
V_{DS} = 30 V; I_{Dq} = 1800 mA.

(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



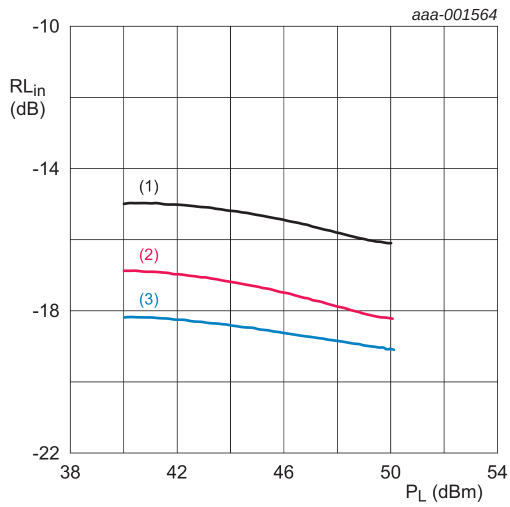
V_{DS} = 30 V; I_{Dq} = 1800 mA.

(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 6. Power gain and drain efficiency as function of output power; typical values



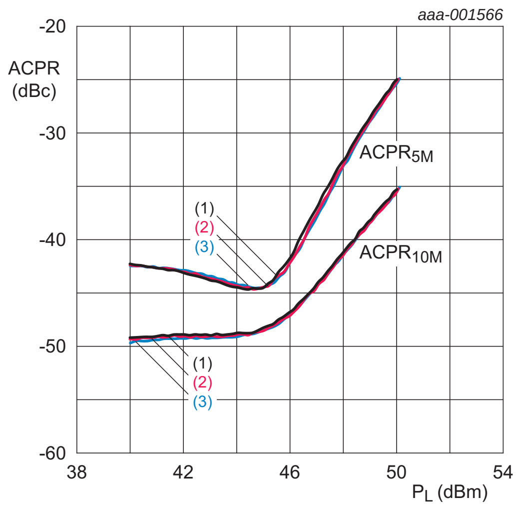
V_{DS} = 30 V; I_{Dq} = 1800 mA.

(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 7. Input return loss as a function of output power; typical values



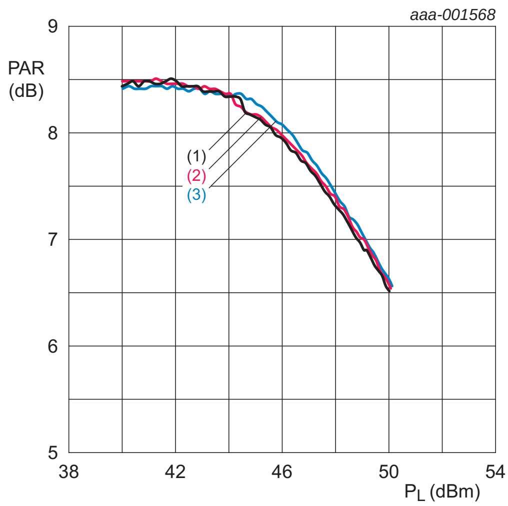
V_{DS} = 30 V; I_{Dq} = 1800 mA.

(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 8. Adjacent channel power ratio (5 MHz and 10 MHz) as function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 1800 mA.

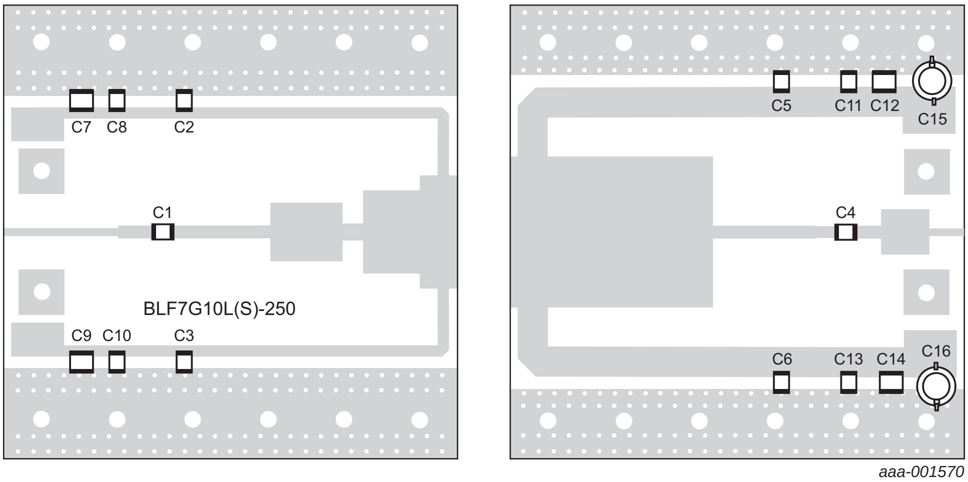
(1) f = 920 MHz

(2) f = 940 MHz

(3) f = 960 MHz

Fig 9. Peak-to-average ratio as a function of output power; typical values

7.5 Circuit



Printed-Circuit Board (PCB): Rogers RO3006; ε_r = 6.15 F/m; thickness = 0.635 mm; thickness copper plating = 35 μm.

The vias can be used as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See Table 9 for list of components.

Fig 10. Component layout

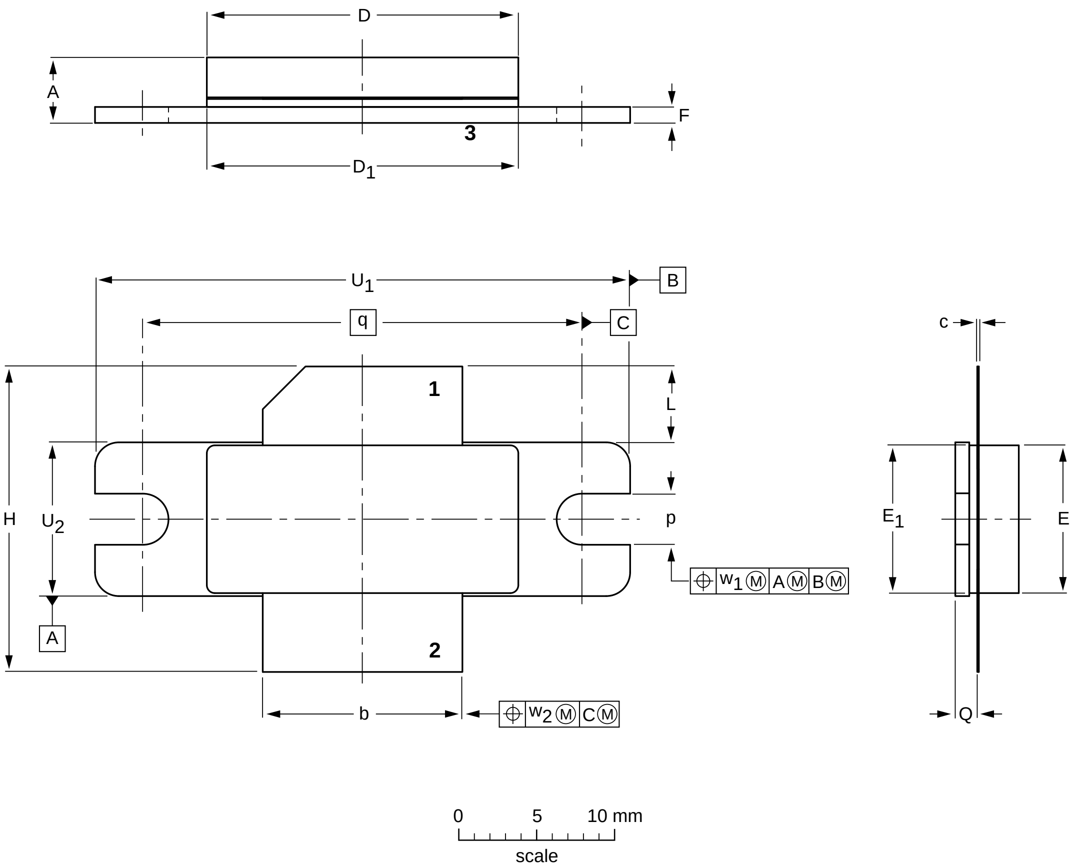
Table 9. List of components

See Figure 10 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	82 pF	ATC800B
C7, C9, C12, C14	multilayer ceramic chip capacitor	10 μF	Murata
C8, C10, C11, C13	multilayer ceramic chip capacitor	1 μF	Murata
C15, C16	electrolytic capacitor	470 μF; 63 V	

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



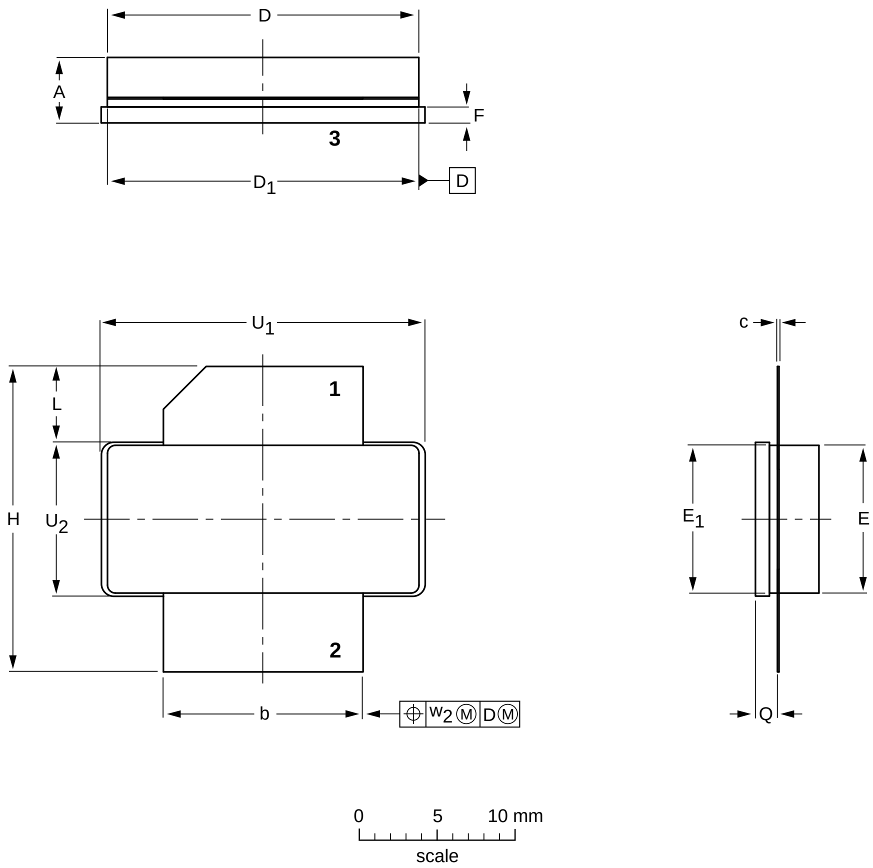
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 11. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~03-01-10~~ 07-05-09

Fig 12. Package outline SOT502B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G10L-250_7G10LS-250 v.3	20120216	Product data sheet	-	BLF7G10L-250_7G10LS-250 v.2
Modifications:	• The status of this data sheet has been changed to Product data sheet • Table 6 on page 3: I_D value changed to 3.3 mA at conditions of $V_{(BR)DSS}$ • Table 8 on page 4: values rounded off to one decimal place			
BLF7G10L-250_7G10LS-250 v.2	20111114	Preliminary data sheet	-	BLF7G10L-250_7G10LS-250 v.1
BLF7G10L-250_7G10LS-250 v.1	20110225	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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Date of release: 16 February 2012

Document identifier: BLF7G10L-250_7G10LS-250