

BLF7G20L-200; BLF7G20LS-200

Power LDMOS transistor

Rev. 4 — 22 July 2011

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 1805 MHz to 1990 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

| Mode of operation | f (MHz) | I_{Dq} (mA) | V_{DS} (V) | $P_{L(AV)}$ (W) | G_p (dB) | η_D (%) | ACPR (dBc) |
|-------------------|--------------|------------------|-----------------|--------------------|---------------|-----------------|-------------------------|
| 2-carrier W-CDMA | 1805 to 1880 | 1620 | 28 | 55 | 18 | 33 | -29 [1] |

[1] Test signal: 3GPP; test model 1; 64 PDPCH; PAR = 8.4 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1805 MHz to 1990 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low-memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

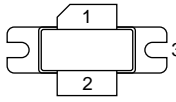
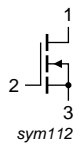
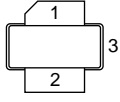
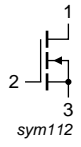
1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi-carrier applications in the 1805 MHz to 1990 MHz frequency range



2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Graphic symbol |
|--------------------------------|-------------|---|---|
| BLF7G20L-200 (SOT502A) | | | |
| 1 | drain |  |  sym112 |
| 2 | gate | | |
| 3 | source | | |
| BLF7G20LS-200 (SOT502B) | | | |
| 1 | drain |  |  sym112 |
| 2 | gate | | |
| 3 | source | | |

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|---------|---|---------|
| | Name | Description | Version |
| BLF7G20L-200 | - | flanged LDMOST ceramic package; 2 mounting holes; 2 leads | SOT502A |
| BLF7G20LS-200 | - | earless flanged LDMOST ceramic package; 2 leads | SOT502B |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|----------------------|------------|------|------|------|
| V_{DS} | drain-source voltage | | - | 65 | V |
| V_{GS} | gate-source voltage | | -0.5 | +13 | V |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | | - | 225 | °C |

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|--|---|------|------|
| $R_{th(j-c)}$ | thermal resistance from junction to case | $T_{case} = 80\text{ °C}; P_L = 55\text{ W}; V_{DS} = 28\text{ V}; I_{Dq} = 1620\text{ mA}$ | 0.27 | K/W |

6. Characteristics

Table 6. Characteristics
T_j = 25 °C unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------------------|--|------|-------|-----|------|
| V _{(BR)DSS} | drain-source breakdown voltage | V _{GS} = 0 V; I _D = 1.5 mA | 65 | - | - | V |
| V _{GS(th)} | gate-source threshold voltage | V _{DS} = 10 V; I _D = 150 mA | 1.5 | 1.9 | 2.3 | V |
| I _{DSS} | drain leakage current | V _{GS} = 0 V; V _{DS} = 28 V | - | - | 4.2 | μA |
| I _{DSX} | drain cut-off current | V _{GS} = V _{GS(th)} + 3.75 V; V _{DS} = 10 V | 42 | 50.6 | - | A |
| I _{GSS} | gate leakage current | V _{GS} = 11 V; V _{DS} = 0 V | -420 | 2.44 | 420 | nA |
| g _{fs} | forward transconductance | V _{DS} = 10 V; I _D = 7.5 A | - | 18.6 | - | S |
| R _{DS(on)} | drain-source on-state resistance | V _{GS} = V _{GS(th)} + 3.75 V; I _D = 5.25 A | - | 0.093 | - | Ω |

7. Test information

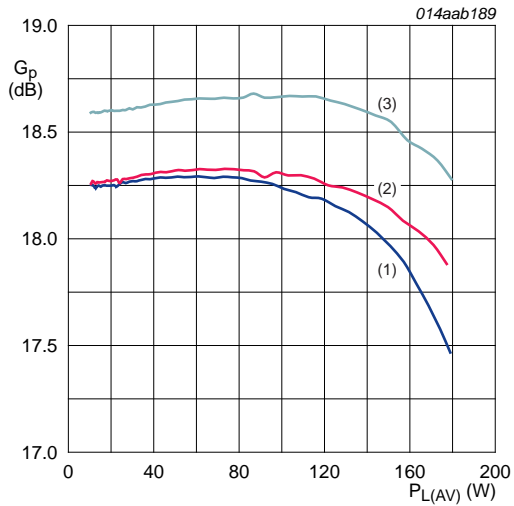
Table 7. Functional test information
Mode of operation: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 PDPCH; f₁ = 1807.5 MHz; f₂ = 1812.5 MHz; f₃ = 1872.5 MHz; f₄ = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1620 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|------------------------------|---------------------------|-----|-----|-----|------|
| P _{L(AV)} | average output power | | - | 55 | - | W |
| G _p | power gain | P _{L(AV)} = 55 W | 17 | 18 | - | dB |
| RL _{in} | input return loss | P _{L(AV)} = 55 W | - | - | -10 | dB |
| η _D | drain efficiency | P _{L(AV)} = 55 W | 30 | 33 | - | % |
| ACPR | adjacent channel power ratio | P _{L(AV)} = 55 W | - | -29 | - | dBc |

7.1 Ruggedness in class-AB operation

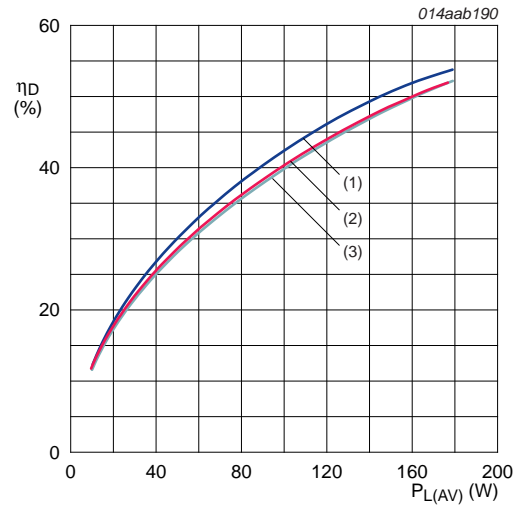
The BLF7G20L-200 and BLF7G20LS-200 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 1620 mA; P_L = 185 W (CW); f = 1805 MHz to 1880 MHz.

7.2 1 Tone CW



$V_{DS} = 28\text{ V}; I_{Dq} = 1620\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1845\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

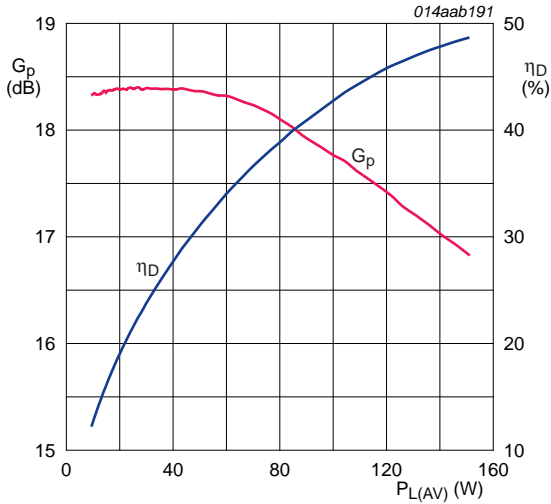
Fig 1. Power gain as a function of average output power; typical values



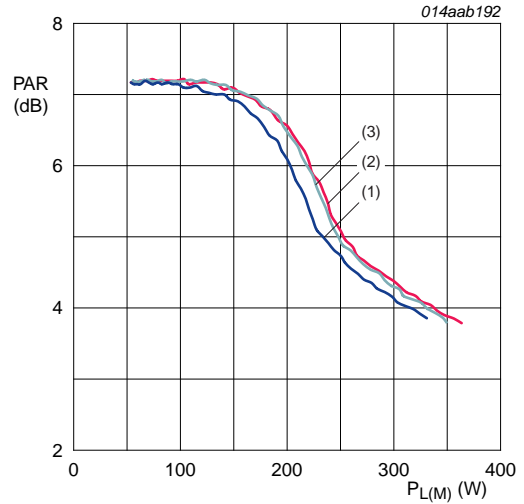
$V_{DS} = 28\text{ V}; I_{Dq} = 1620\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1845\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 2. Drain efficiency as a function of average output power; typical values

7.3 1-carrier W-CDMA



$V_{DS} = 28\text{ V}$; $I_{DQ} = 1620\text{ mA}$; $f = 1845\text{ MHz}$; $PAR = 7.2\text{ dB}$ at 0.01 % probability on the CCDF.

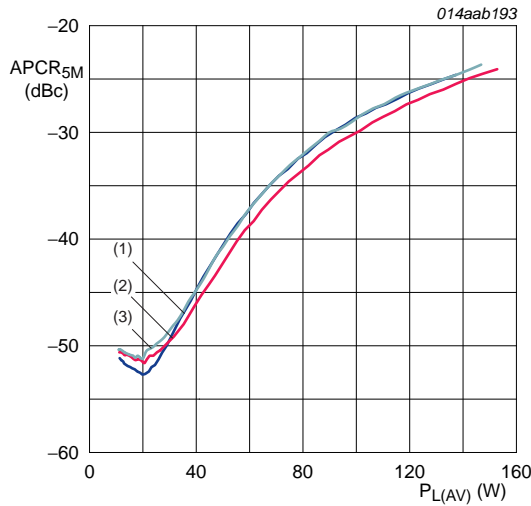


$V_{DS} = 28\text{ V}$; $I_{DQ} = 1620\text{ mA}$; $PAR = 7.2\text{ dB}$ at 0.01 % probability on the CCDF.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1845\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 3. Power gain and drain efficiency as functions of average output power; typical values

Fig 4. Peak-to-average power ratio as a function of peak power; typical values

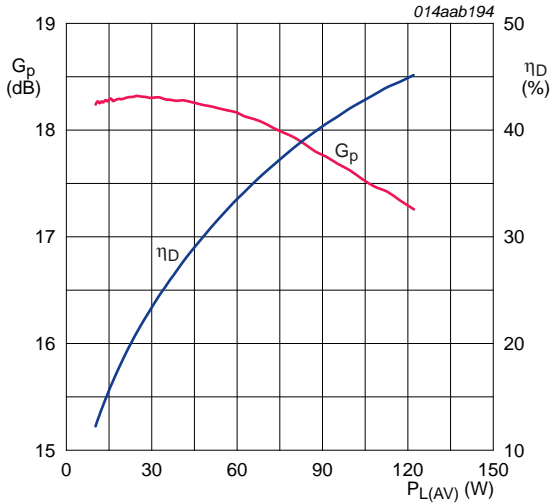


$V_{DS} = 28\text{ V}$; $I_{DQ} = 1620\text{ mA}$; $PAR = 7.2\text{ dB}$ at 0.01 % probability on the CCDF.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1845\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

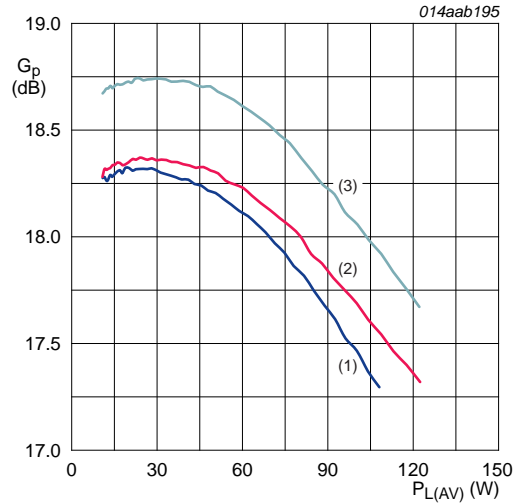
Fig 5. Adjacent power channel ratio (5 MHz) as function of average output power; typical values

7.4 2-carrier W-CDMA



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$; channel spacing = 5 MHz;
 PAR = 8.4 dB at 0.01 % probability on the CCDF.

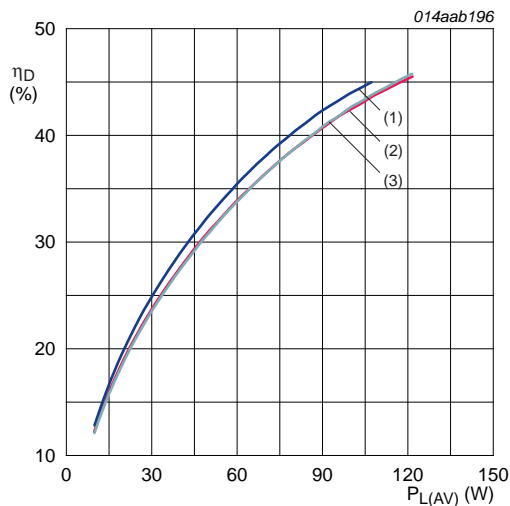
Fig 6. Power gain and drain efficiency as functions of average output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$; channel spacing = 5 MHz;
 PAR = 8.4 dB at 0.01 % probability on the CCDF.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1845\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

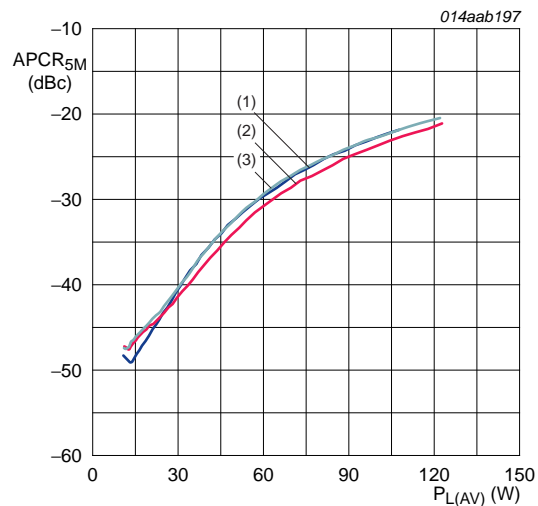
Fig 7. Power gain as a function of average output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$; channel spacing = 5 MHz;
 PAR = 8.4 dB at 0.01 % probability on the CCDF.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1845\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 8. Drain efficiency as a function of average output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$; channel spacing = 5 MHz;
 PAR = 8.4 dB at 0.01 % probability on the CCDF.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1845\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 9. Adjacent power channel ratio (5 MHz) as a function of average output power; typical values

7.5 Test circuit

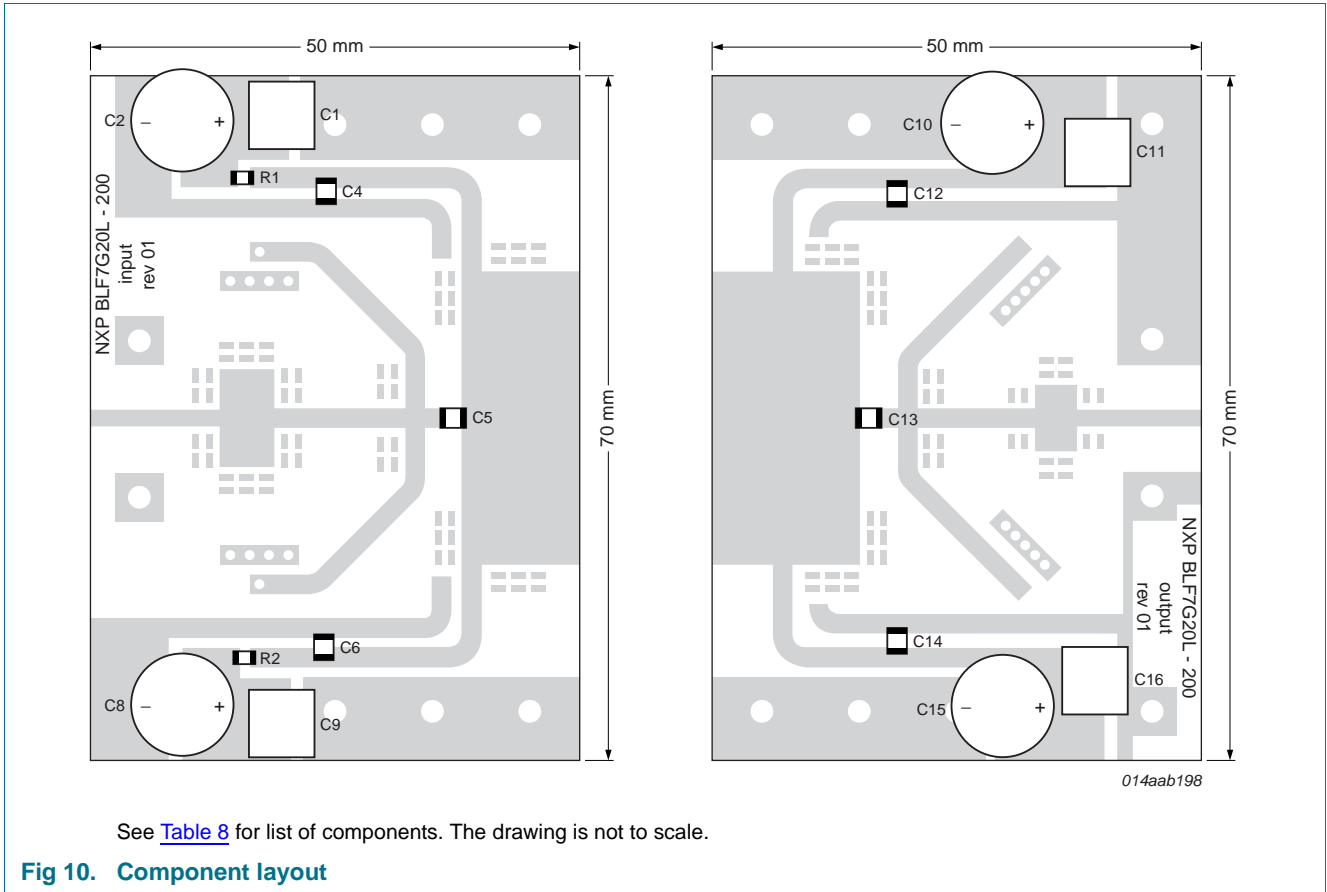


Table 8. List of components

See [Figure 10](#) for component layout.

| Component | Description | Value | Remarks |
|------------------|-----------------------------------|-------------------|--------------|
| C1, C9, C11, C16 | multilayer ceramic chip capacitor | 10 μ F | TDK |
| C4, C6 | multilayer ceramic chip capacitor | 68 pF | ATC800B |
| C5 | multilayer ceramic chip capacitor | 2.0 pF | ATC800B |
| C12, C14 | multilayer ceramic chip capacitor | 100 pF | ATC800B |
| C13 | multilayer ceramic chip capacitor | 3.3 pF | ATC800B |
| C2, C8, C10, C15 | electrolytic capacitor | 470 μ F; 63 V | |
| R1, R2 | chip resistor | 10 Ω | Philips 0603 |

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

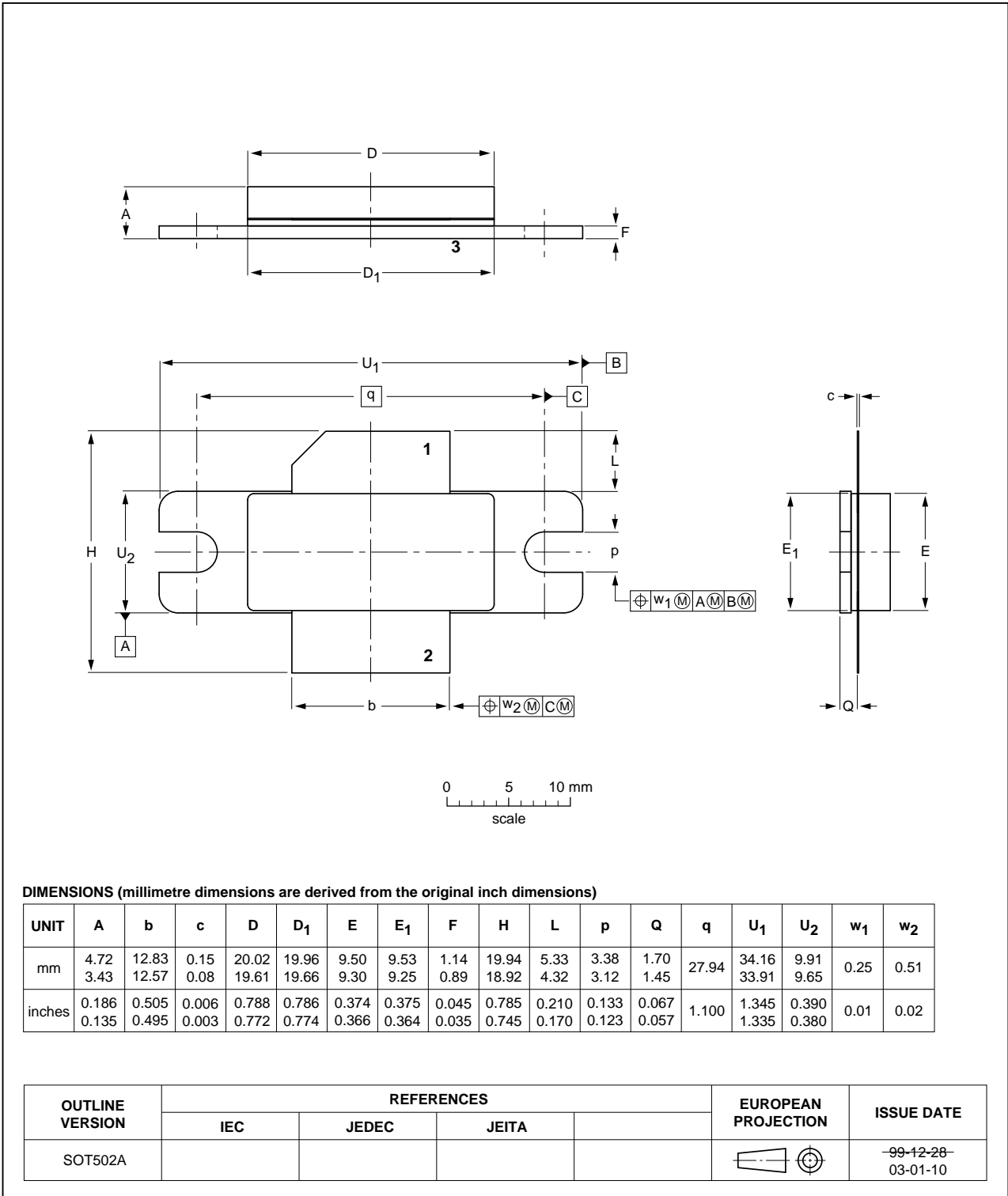


Fig 11. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

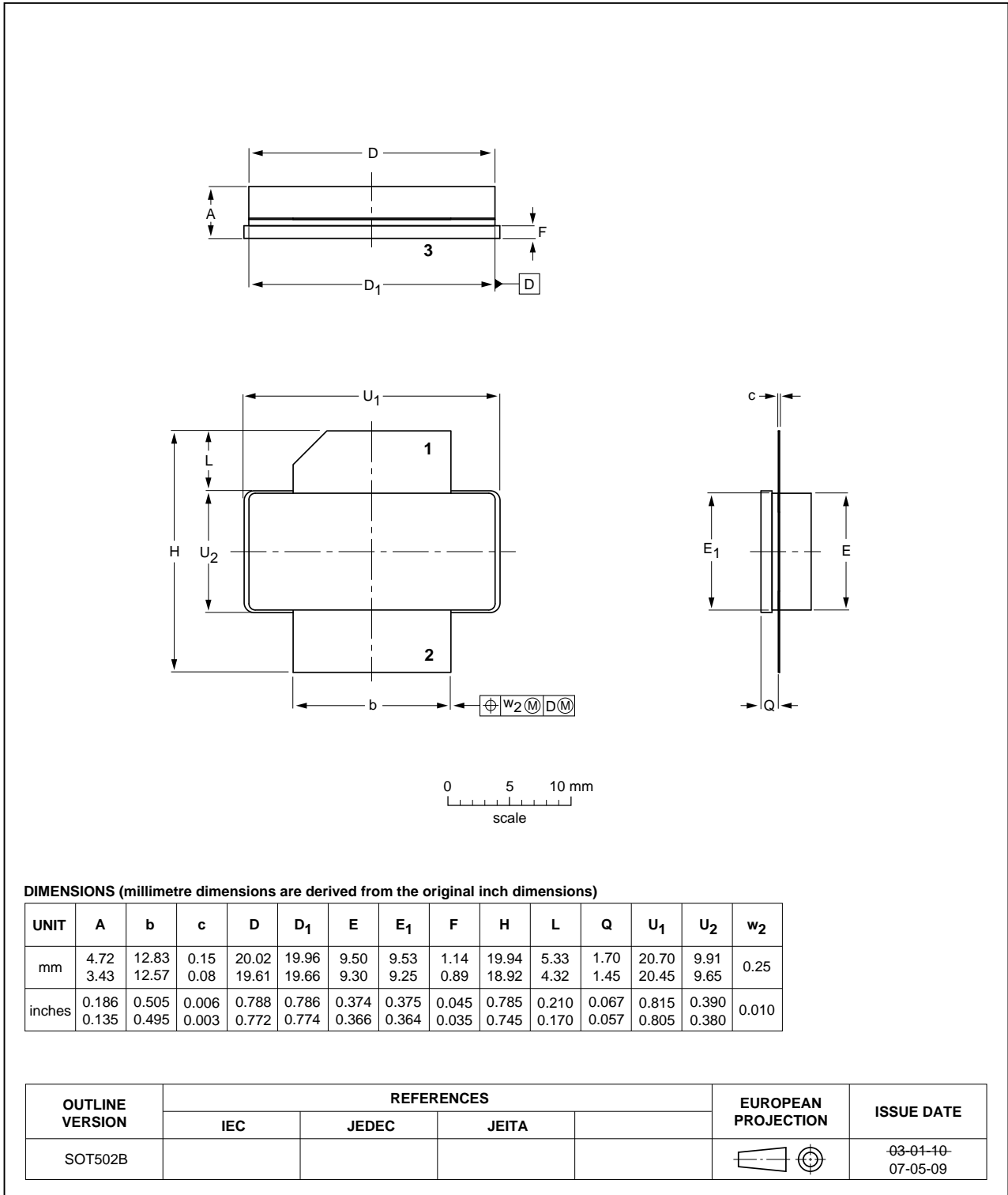


Fig 12. Package outline SOT502B

9. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| 3GPP | Third Generation Partnership Project |
| CCDF | Complementary Cumulative Distribution Function |
| CW | Continuous Wave |
| DPCH | Dedicated Physical CHannel |
| ESD | ElectroStatic Discharge |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| LDMOST | Laterally Diffused Metal Oxide Semiconductor Transistor |
| PAR | Peak-to-Average power Ratio |
| PDPCH | transmission Power of the Dedicated Physical CHannel |
| RF | Radio Frequency |
| VSWR | Voltage Standing Wave Ratio |
| W-CDMA | Wideband Code Division Multiple Access |

10. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------------|---|------------------------|---------------|-----------------------------|
| BLF7G20L-200_7G20LS-200 v.4 | 20110722 | Product data sheet | - | BLF7G20L-200_7G20LS-200 v.3 |
| Modifications: | <ul style="list-style-type: none"> The status of this document has been changed to Product data sheet. | | | |
| BLF7G20L-200_7G20LS-200 v.3 | 20110301 | Preliminary data sheet | - | BLF7G20L-200_7G20LS-200 v.2 |
| BLF7G20L-200_7G20LS-200 v.2 | 20100827 | Preliminary data sheet | - | BLF7G20L-200_7G20LS-200 v.1 |
| BLF7G20L-200_7G20LS-200 v.1 | 20100603 | Objective data sheet | - | - |

11. Legal information

11.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

11.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

11.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

11.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

13. Contents

| | | |
|-----------|--|-----------|
| 1 | Product profile | 1 |
| 1.1 | General description | 1 |
| 1.2 | Features and benefits | 1 |
| 1.3 | Applications | 1 |
| 2 | Pinning information | 2 |
| 3 | Ordering information | 2 |
| 4 | Limiting values | 2 |
| 5 | Thermal characteristics | 2 |
| 6 | Characteristics | 3 |
| 7 | Test information | 3 |
| 7.1 | Ruggedness in class-AB operation | 3 |
| 7.2 | 1 Tone CW | 4 |
| 7.3 | 1-carrier W-CDMA | 5 |
| 7.4 | 2-carrier W-CDMA | 6 |
| 7.5 | Test circuit | 7 |
| 8 | Package outline | 8 |
| 9 | Abbreviations | 10 |
| 10 | Revision history | 10 |
| 11 | Legal information | 11 |
| 11.1 | Data sheet status | 11 |
| 11.2 | Definitions | 11 |
| 11.3 | Disclaimers | 11 |
| 11.4 | Trademarks | 12 |
| 12 | Contact information | 12 |
| 13 | Contents | 13 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011. All rights reserved.

For more information, please visit: <http://www.nxp.com>
 For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 22 July 2011

Document identifier: BLF7G20L-200_7G20LS-200