BLF7G21L-160P; BLF7G21LS-160P

Power LDMOS transistor

Rev. 2 — 13 October 2011 Product data sheet

1. Product profile

1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2050 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	1930 to 1990	1080	28	45	18	34	–30[1]
1-carrier W-CDMA	1930 to 1990	1080	28	50	18.0	36	–34[2]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

[2] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

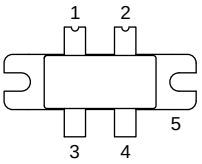
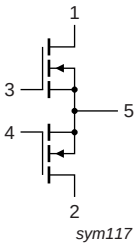
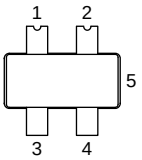
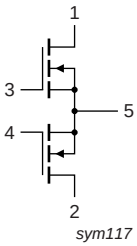
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1800 MHz to 2050 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1800 MHz to 2050 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF7G21L-160P (SOT1121A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLF7G21LS-160P (SOT1121B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G21L-160P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF7G21LS-160P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	32.5	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 100 W	0.41	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 90 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	14	-	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	200	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 4.5 A	-	7	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.15 A	-	0.15	-	Ω

7. Test information

Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 PDPCH; f_1 = 1932.5 MHz; f_2 = 1937.5 MHz; f_3 = 1982.5 MHz; f_4 = 1987.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1080 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 45 W	17.0	18.0	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 45 W	-	–15	–8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 45 W	31	34	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 45 W		–30	–25	dBc
$ACPR_{10M}$	adjacent channel power ratio (10 MHz)	$P_{L(AV)}$ = 45 W	-	-	-	dBc

Table 8. Application information

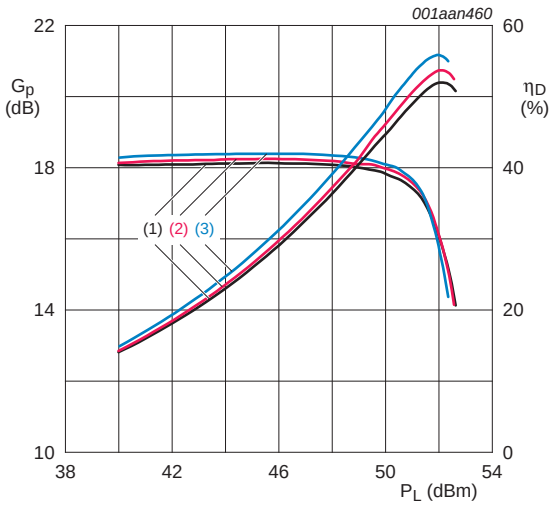
Mode of operation: 1-carrier W-CDMA; PAR 7.2 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 PDPCH; f_1 = 1932.5 MHz; f_2 = 1987.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1080 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 80 W; at 0.01 % probability on CCDF	4.0	4.5	-	dB

7.1 Ruggedness in class-AB operation

The BLF7G21L-160P and BLF7G21LS-160P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1080 mA; P_L = 160 W (CW); f = 1805 MHz.

7.2 CW



V_{DS} = 28 V; I_{Dq} = 1080 mA.

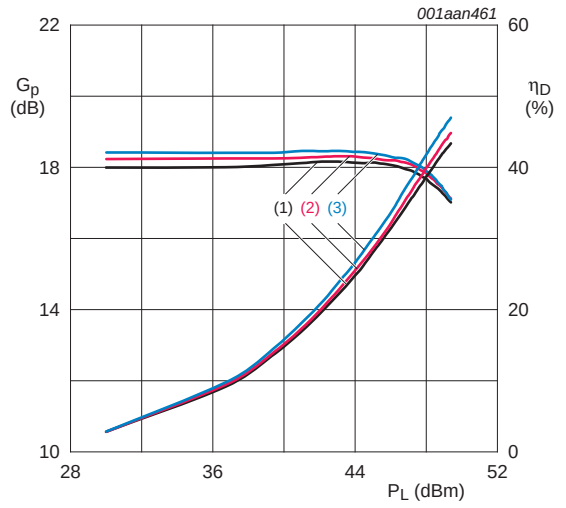
(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 1. Power gain and drain efficiency as function of load power; typical values

7.3 1-Carrier W-CDMA



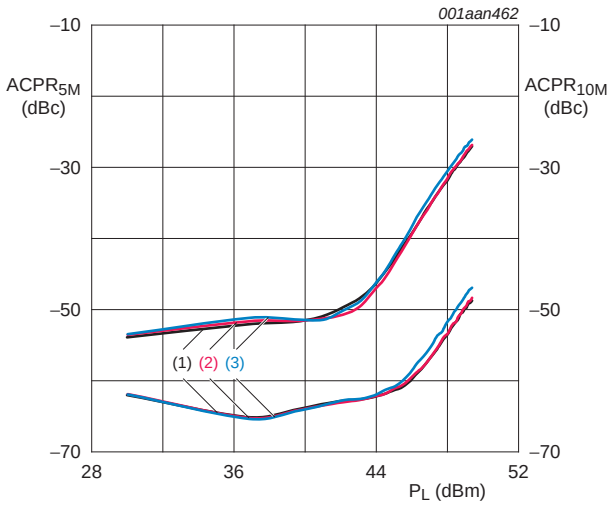
V_{DS} = 28 V; I_{Dq} = 1080 mA.

(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 2. Power gain and drain efficiency as function of load power; typical values



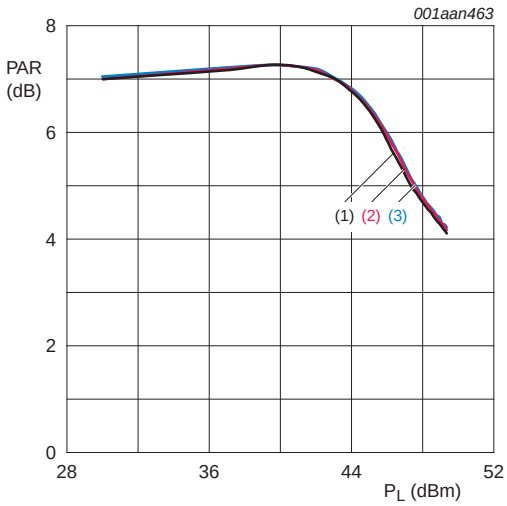
V_{DS} = 28 V; I_{Dq} = 1080 mA.

(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 3. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1080 mA.

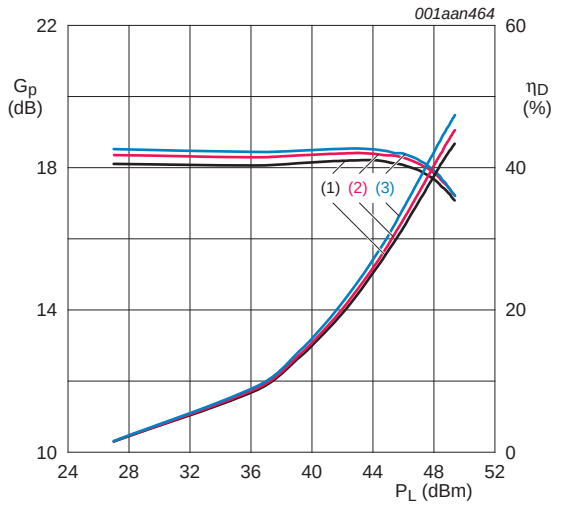
(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 4. Peak-to-average ratio as a function of load power; typical values

7.4 2-Carrier W-CDMA 5 MHz



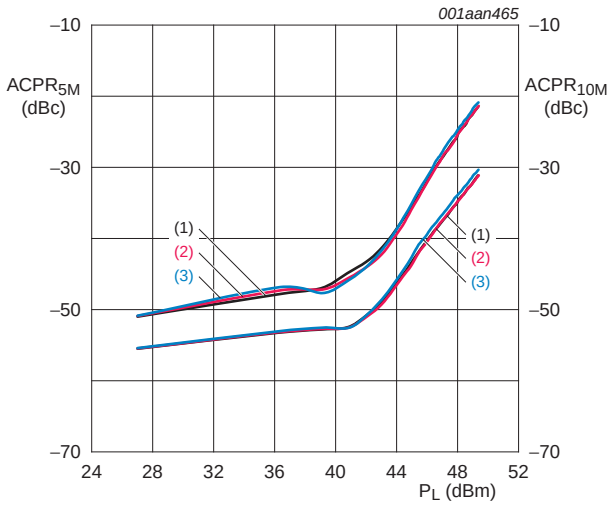
V_{DS} = 28 V; I_{Dq} = 1080 mA.

(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 5. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1080 mA.

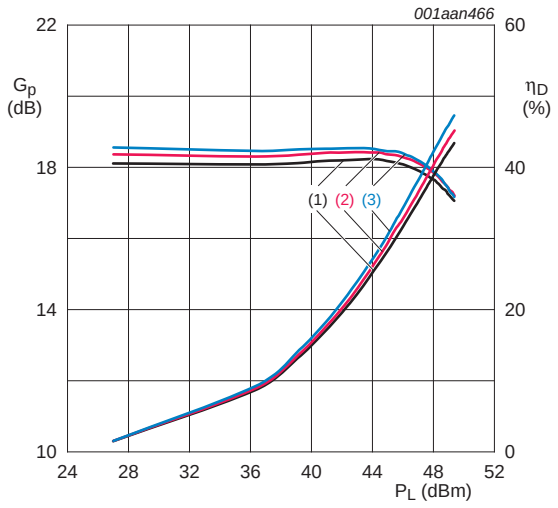
(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 6. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as a function of load power; typical values

7.5 2-Carrier W-CDMA 10 MHz



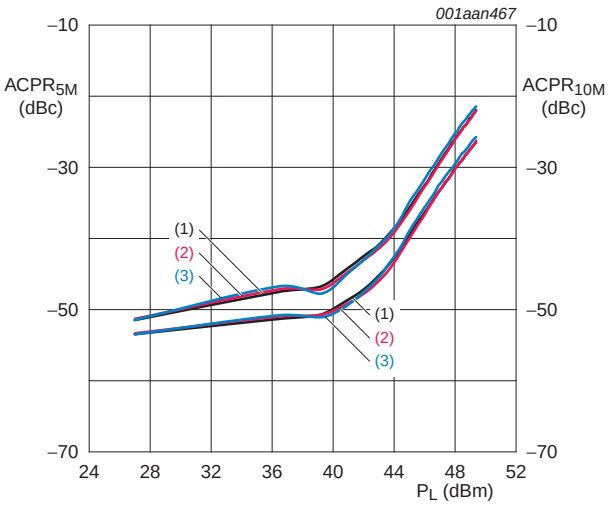
V_{DS} = 28 V; I_{Dq} = 1080 mA.

(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 7. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1080 mA.

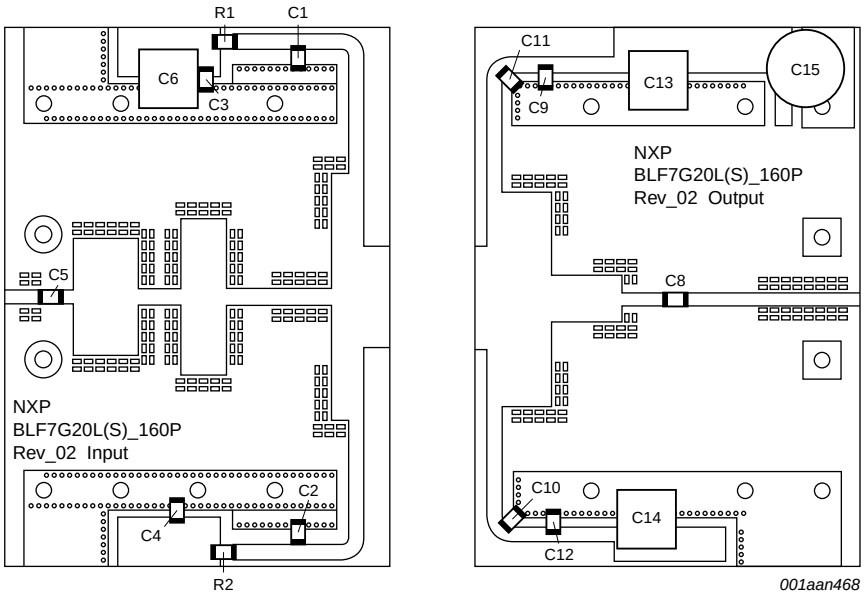
(1) f = 1930 MHz

(2) f = 1960 MHz

(3) f = 1990 MHz

Fig 8. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as a function of load power; typical values

7.6 Test circuit



Printed-Circuit Board (PCB): Taconic RF35; ε_r = 3.5; thickness = 0.76 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 9. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 9.

Component	Description	Value		Remarks
C1, C2, C5, C9, C10	multilayer ceramic chip capacitor	68 pF	[1]	
C3, C4, C11, C12	multilayer ceramic chip capacitor	820 pF	[2]	
C6, C13, C14	multilayer ceramic chip capacitor	10 μF	[3]	
C8	multilayer ceramic chip capacitor	10 pF	[1]	
C15	electrolytic capacitor	470 μF; 63 V		
R1, R2	SMD resistor	12 Ω		Philips 1206

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] TDK or capacitor of same quality.

7.7 Impedance information

Table 10. Typical impedance

Typical values valid for both section in parallel unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
1750	0.99 – j4.09	2.32 – j2.35
1805	1.12 – j4.39	2.20 – j2.20
1840	1.23 – j4.58	2.08 – j2.14
1880	1.31 – j4.74	1.94 – j2.12
1930	1.49 – j5.01	1.76 – j2.15
1960	1.61 – j5.19	1.66 – j2.20
1990	1.75 – j5.36	1.56 – j2.26
2020	1.91 – j5.54	1.48 – j2.34
2050	2.13 – j5.75	1.4 – j2.42

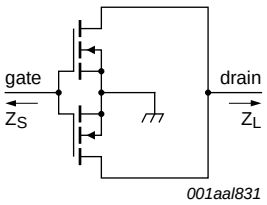
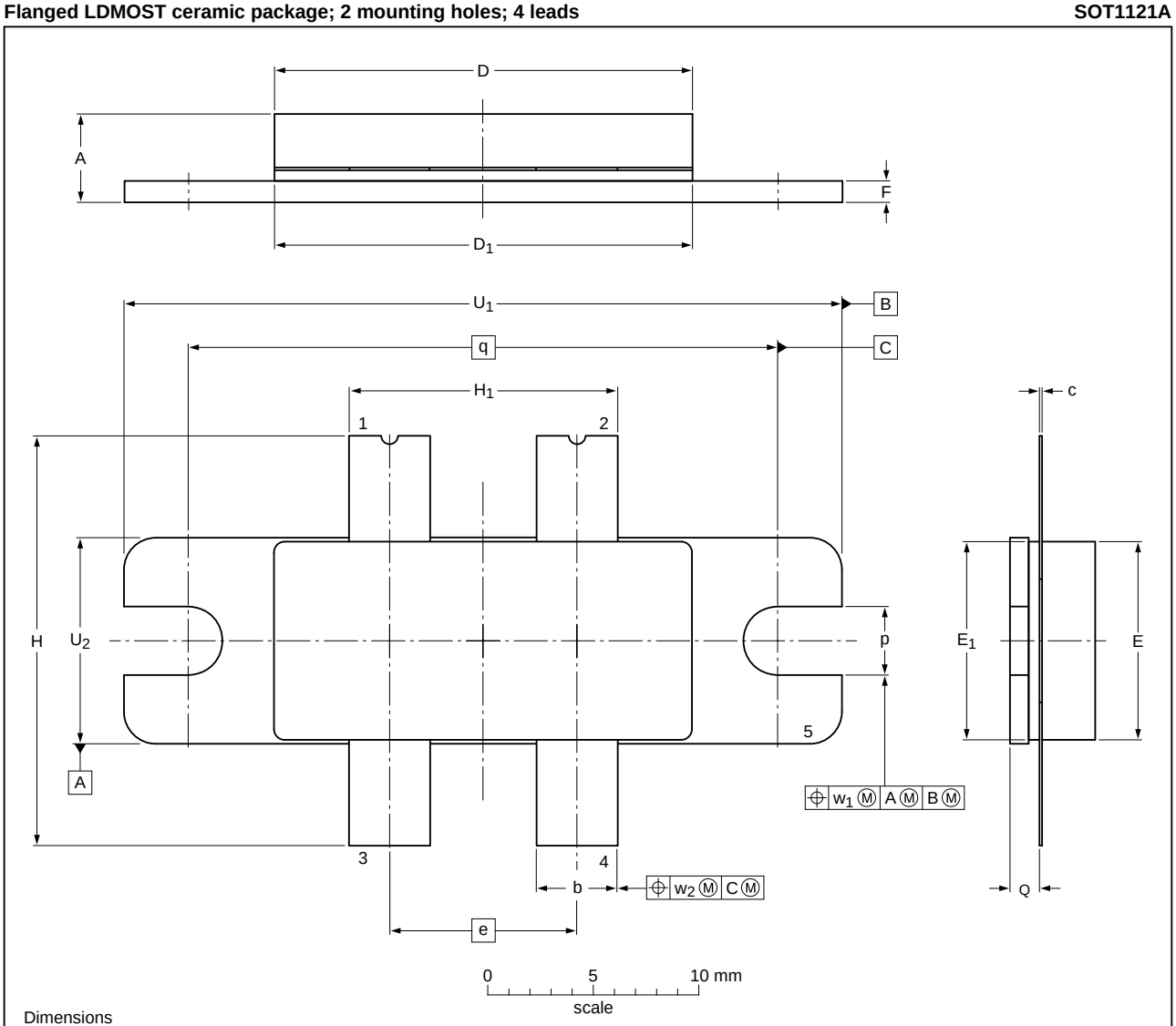


Fig 10. Definition of transistor impedance

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1121A**



Dimensions

Unit[1]		A	b	c	D	D1	e	E	E1	F	H	H1	p	Q[2]	q	U1	U2	w1	w2
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70		34.16	9.91		
	nom						8.89								27.94			0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66		9.27	9.27	0.89	18.92	12.57	3.12	1.45		33.91	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067		1.345	0.39		
	nom						0.35								1.1			0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.123	0.057		1.335	0.38		

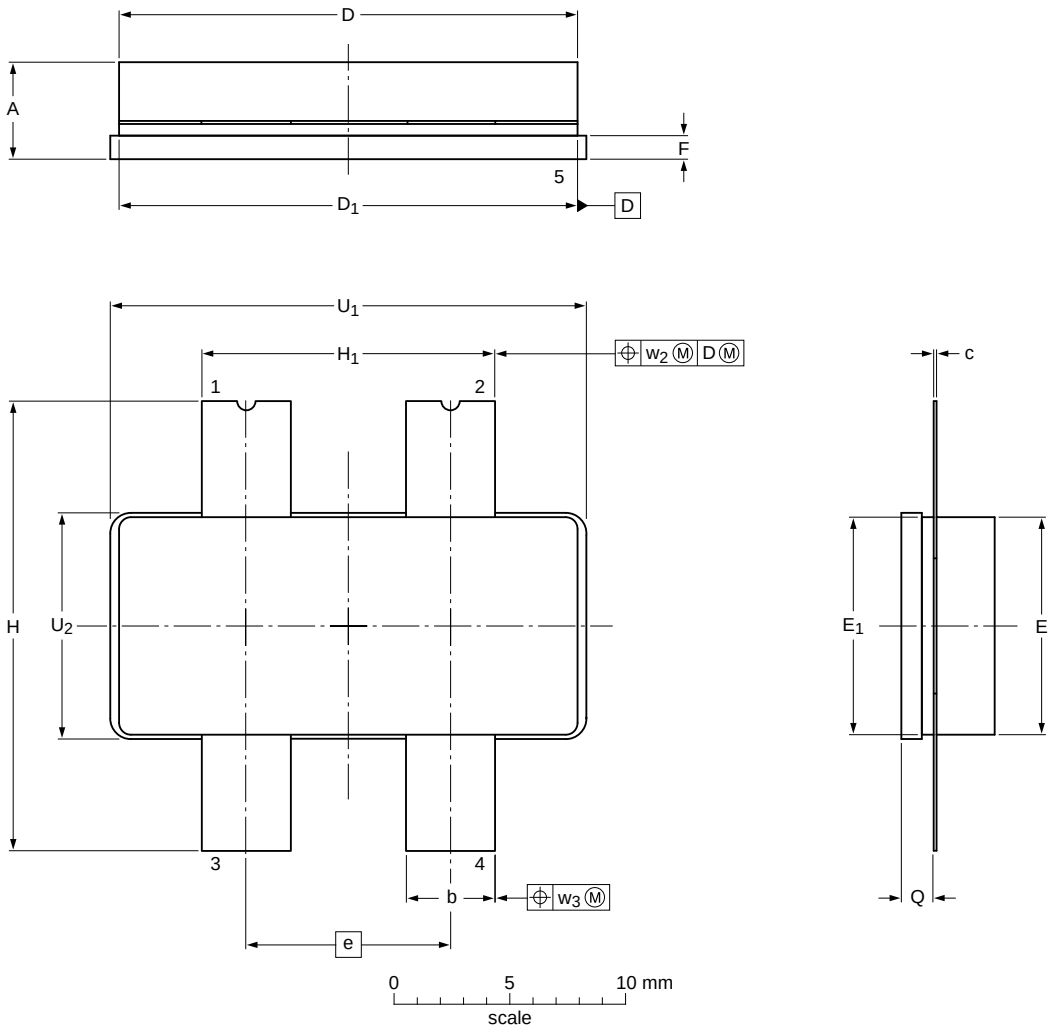
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121A						~~09-10-12~~ 10-02-02

Fig 11. Package outline SOT1121A

Earless flanged LDMOST ceramic package; 4 leads **SOT1121B**



Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q	U_1	U_2	w_2	w_3
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91		
	nom						8.89									0.51	0.25
	min	3.45	3.68	0.08	19.61	19.66		9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39		
	nom						0.35									0.02	0.01
	min	0.136	0.145	0.003	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38		

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121B						~~09-10-12~~ 09-12-14

Fig 12. Package outline SOT1121B

9. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G21L-160P_7G21LS-160P v.2	20111013	Product data sheet	-	BLF7G21L-160P_7G21LS-160P v.1
Modifications:	• The status of this document has been changed to Product data sheet.			
BLF7G21L-160P_7G21LS-160P v.1	20110401	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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