

BLF8G20LS-220

Power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

220 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

| Test signal | f (MHz) | I_{Dq} (mA) | V_{DS} (V) | $P_{L(AV)}$ (W) | G_p (dB) | η_D (%) | ACPR (dBc) |
|------------------|--------------|------------------|-----------------|--------------------|---------------|-----------------|-------------------------|
| 2-carrier W-CDMA | 1805 to 1880 | 1600 | 28 | 55 | 18.9 | 34 | -31 [1] |

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

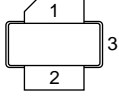
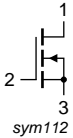
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Graphic symbol |
|-----|----------------------------|---|---|
| 1 | drain |  |  sym112 |
| 2 | gate | | |
| 3 | source [1] | | |

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|---------|--|---------|
| | Name | Description | Version |
| BLF8G20LS-220 | - | earless flanged ceramic package; 2 leads | SOT502B |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|----------------------|------------|-----------------------|------|------|
| V_{DS} | drain-source voltage | | - | 65 | V |
| V_{GS} | gate-source voltage | | -0.5 | +13 | V |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | | [1] - | 225 | °C |

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|--|--|------|------|
| $R_{th(j-c)}$ | thermal resistance from junction to case | $T_{case} = 80\text{ °C}; P_L = 55\text{ W};$ $V_{DS} = 28\text{ V}; I_{Dq} = 1600\text{ mA}$ | 0.27 | K/W |

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|---|-----|-------|-----|---------------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS} = 0\text{ V}; I_D = 2.7\text{ mA}$ | 65 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$ | 1.5 | 1.9 | 2.3 | V |
| V_{GSq} | gate-source quiescent voltage | $V_{DS} = 28\text{ V}; I_D = 1.6\text{ A}$ | 1.7 | 2.1 | 2.5 | V |
| I_{DSS} | drain leakage current | $V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$ | - | - | 4.2 | μA |
| I_{DSX} | drain cut-off current | $V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$ | - | 50.6 | - | A |
| I_{GSS} | gate leakage current | $V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$ | - | - | 420 | nA |
| g_{fs} | forward transconductance | $V_{DS} = 10\text{ V}; I_D = 13.5\text{ A}$ | - | 19.6 | - | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 9.45\text{ A}$ | - | 0.057 | - | Ω |

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; $f_1 = 1807.5\text{ MHz}; f_2 = 1812.5\text{ MHz}; f_3 = 1872.5\text{ MHz}; f_4 = 1877.5\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 1600\text{ mA}; T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a production circuit.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|------------------------------|---------------------------|------|-------|-----|------|
| G_p | power gain | $P_{L(AV)} = 55\text{ W}$ | 17.8 | 18.9 | - | dB |
| η_D | drain efficiency | $P_{L(AV)} = 55\text{ W}$ | 29 | 34 | - | % |
| RL_{in} | input return loss | $P_{L(AV)} = 55\text{ W}$ | - | -15.5 | -7 | dB |
| ACPR | adjacent channel power ratio | $P_{L(AV)} = 55\text{ W}$ | - | -31 | -26 | dBc |

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G20LS-220 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}; I_{Dq} = 1600\text{ mA}; P_L = 200\text{ W (CW)}; f = 1805\text{ MHz}$.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data; $I_{Dq} = 1600\text{ mA}; V_{DS} = 28\text{ V}$.

| f (MHz) | Z_S [1] (Ω) | Z_L [1] (Ω) |
|---------|------------------------|------------------------|
| 1805 | 1.38 – j3.45 | 0.90 – j2.50 |
| 1843 | 1.43 – j3.63 | 0.82 – j2.37 |
| 1880 | 1.38 – j3.56 | 0.90 – j2.60 |

[1] Z_S and Z_L defined in [Figure 1](#).

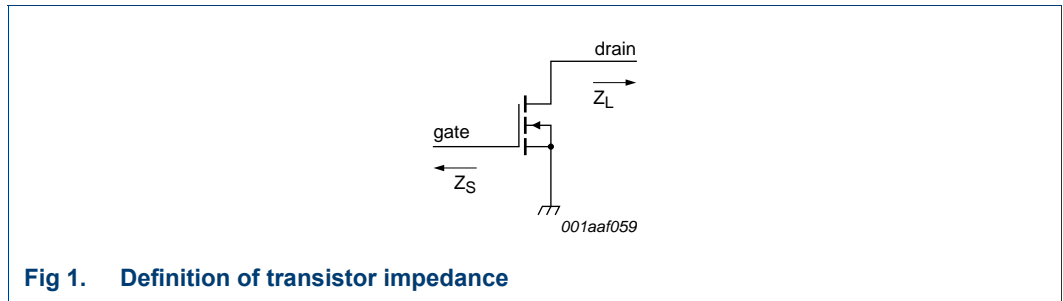
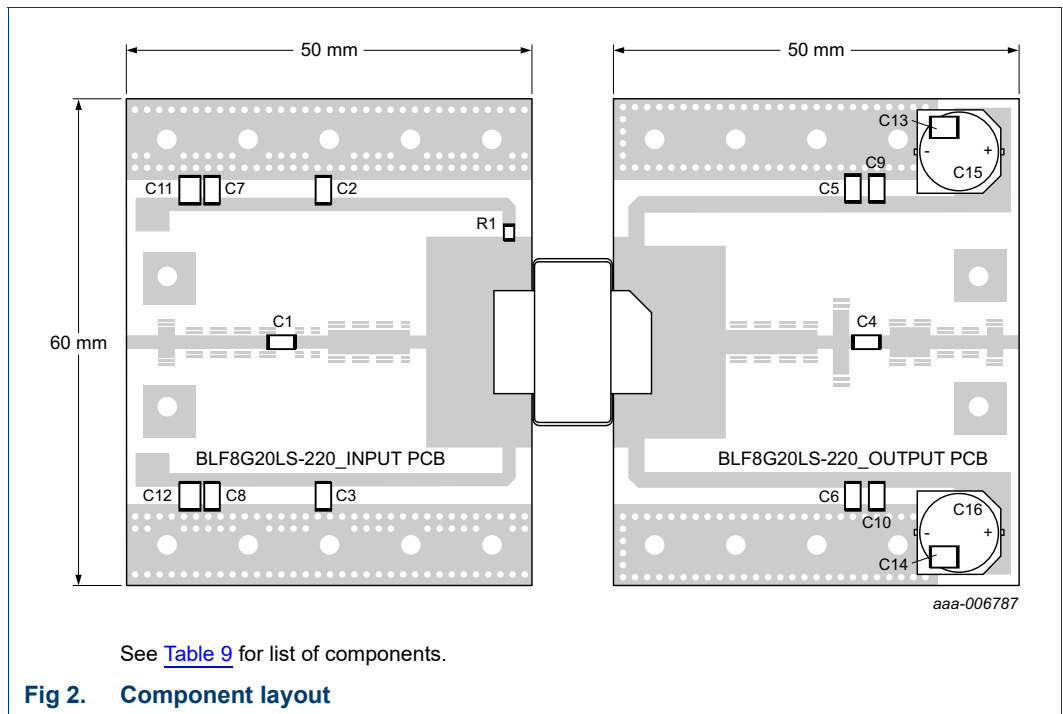


Fig 1. Definition of transistor impedance

7.3 Test circuit



See [Table 9](#) for list of components.

Fig 2. Component layout

Table 9. List of components

See [Figure 2](#) for component layout.

The used PCB material is Rogers RO4350B with a thickness of 0.76 mm.

| Component | Description | Value | Remarks |
|------------------------|-----------------------------------|-------------------|-------------|
| C1, C2, C3, C4, C5, C6 | multilayer ceramic chip capacitor | 33 pF | [1] ATC100B |
| C7, C8, C9, C10 | multilayer ceramic chip capacitor | 1 μ F | [2] TDK |
| C11, C12, C13, C14 | multilayer ceramic chip capacitor | 10 μ F | [3] Murata |
| C15, C16 | multilayer ceramic chip capacitor | 470 μ F, 63 V | |
| R1 | chip resistor | 9.1 Ω | SMD 0805 |

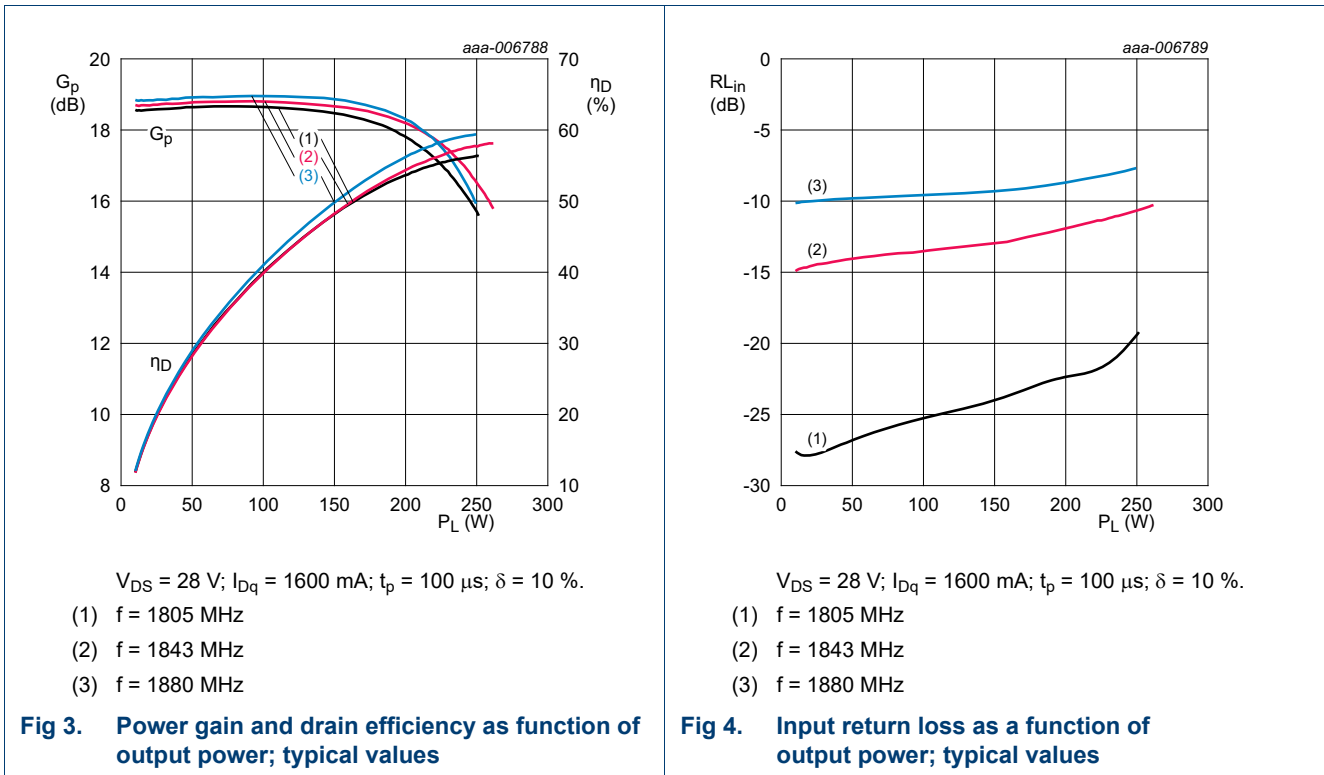
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] TDK or capacitor of same quality.

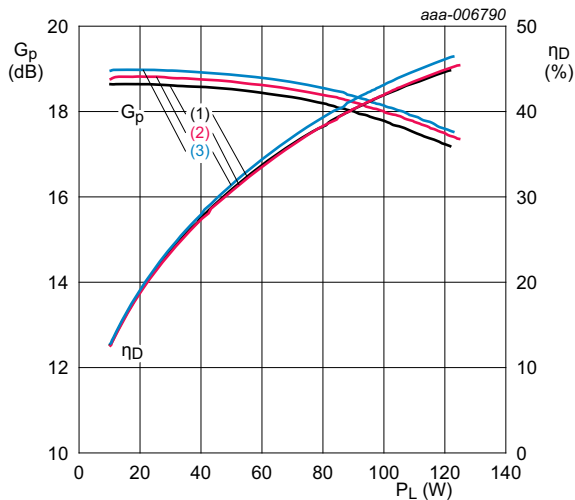
[3] Murata or capacitor of same quality.

7.4 Graphical data

7.4.1 CW pulse

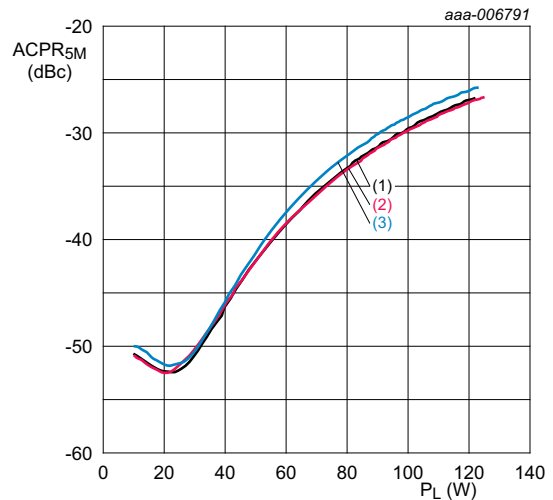


7.4.2 1-Carrier W-CDMA



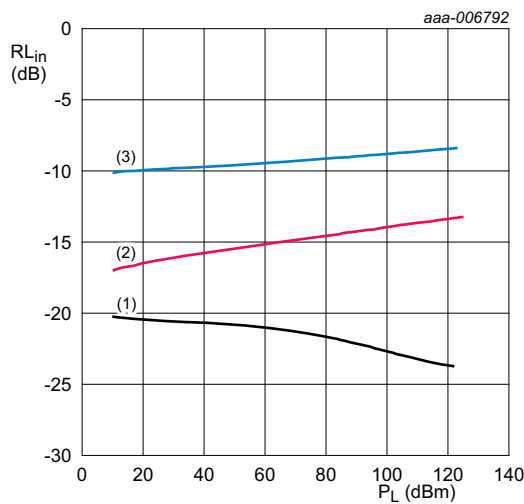
$V_{DS} = 28\text{ V}; I_{Dq} = 1600\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1843\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 1600\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1843\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

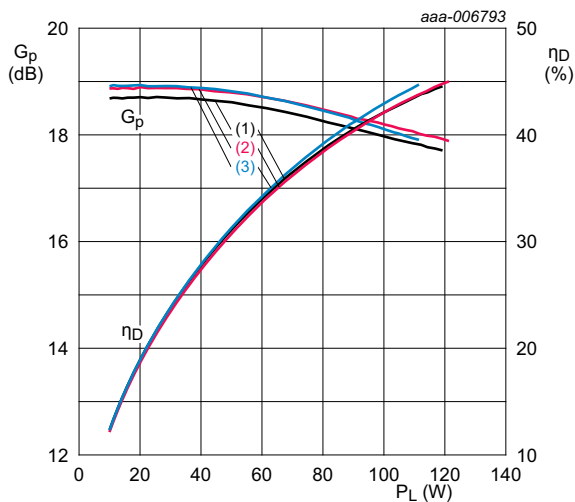
Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 1600\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1843\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 7. Input return loss as a function of output power; typical values

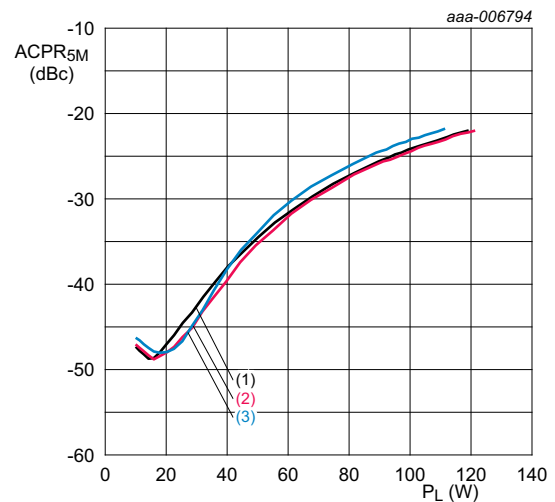
7.4.3 2-Carrier W-CDMA



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1600\text{ mA}$; $f = 5\text{ MHz}$; $\delta = 46\%$.

- (1) $f = 1810\text{ MHz}$
- (2) $f = 1843\text{ MHz}$
- (3) $f = 1877.5\text{ MHz}$

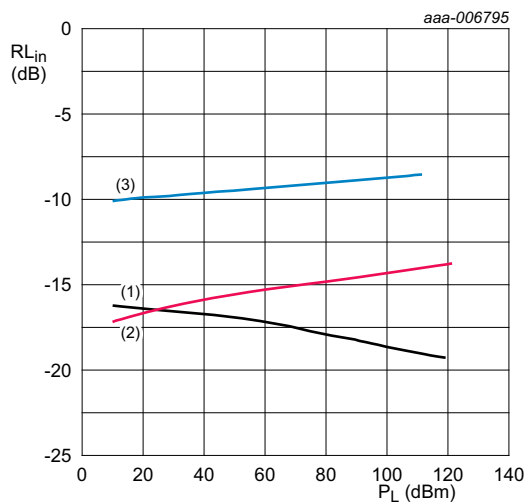
Fig 8. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1600\text{ mA}$; $f = 5\text{ MHz}$; $\delta = 46\%$.

- (1) $f = 1810\text{ MHz}$
- (2) $f = 1843\text{ MHz}$
- (3) $f = 1877.5\text{ MHz}$

Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1600\text{ mA}$; $f = 5\text{ MHz}$; $\delta = 46\%$.

- (1) $f = 1810\text{ MHz}$
- (2) $f = 1843\text{ MHz}$
- (3) $f = 1877.5\text{ MHz}$

Fig 10. Input return loss as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 2 leads

SOT502B

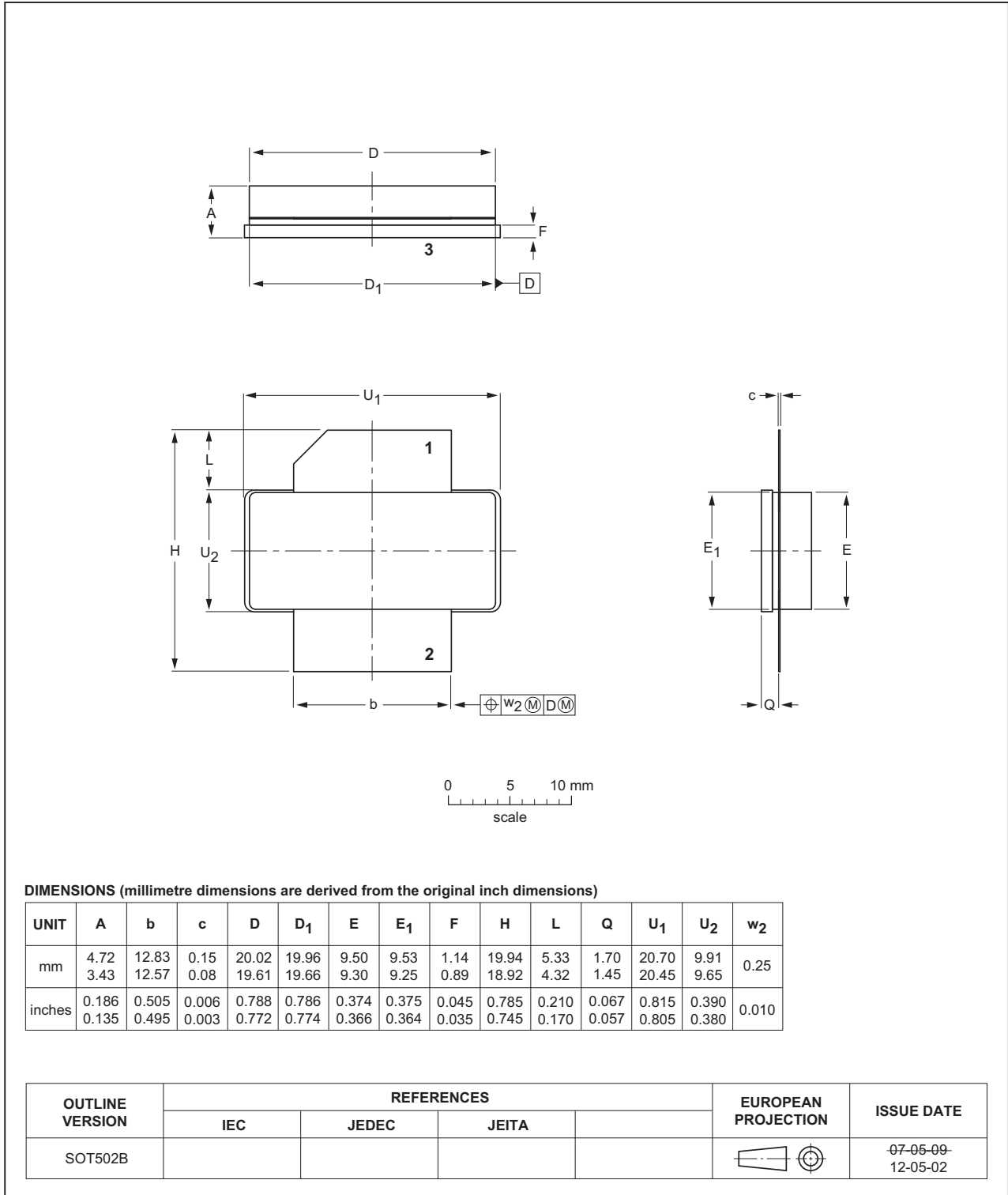


Fig 11. Package outline SOT502B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| 3GPP | 3rd Generation Partnership Project |
| CCDF | Complementary Cumulative Distribution Function |
| CW | Continuous Wave |
| DPCH | Dedicated Physical CHannel |
| ESD | ElectroStatic Discharge |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| PAR | Peak-to-Average Ratio |
| SMD | Surface Mounted Device |
| VSWR | Voltage Standing Wave Ratio |
| W-CDMA | Wideband Code Division Multiple Access |

11. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|----------------------|---------------|-------------------|
| BLF8G20LS-220#3 | 20150901 | Product data sheet | | BLF8G20LS-220 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. | | | |
| BLF8G20LS-220 v.2 | 20130530 | Product data sheet | - | BLF8G20LS-220 v.1 |
| BLF8G20LS-220 v.1 | 20130307 | Objective data sheet | - | - |

12. Legal information

12.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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