

BLF8G24LS-200PN

Power LDMOS transistor

Rev. 3 — 1 December 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Test signal	f	I_{DQ}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2300 to 2400	1740	28	60	17.2	32	-37 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

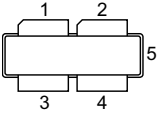
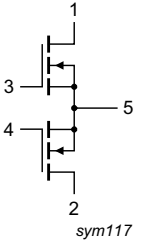
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source ^[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G24LS-200PN	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C
T_{case}	case temperature		^[1] -	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 60\text{ W}$	0.217	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 100\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	26.8	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 5.1\text{ A}$	-	1.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5.04\text{ A}$	-	0.1	-	Ω

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; $f_1 = 2300\text{ MHz}; f_2 = 2400\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 1740\text{ mA}; T_{case} = 25\text{ °C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 60\text{ W}$	15.8	17.2	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 60\text{ W}$	-	-11	-8	dB
η_D	drain efficiency	$P_{L(AV)} = 60\text{ W}$	27	32	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 60\text{ W}$	-	-37	-34	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G24LS-200PN is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}; I_{Dq} = 1740\text{ mA}; P_L = 200\text{ W (CW)}; f = 2300\text{ MHz}$.

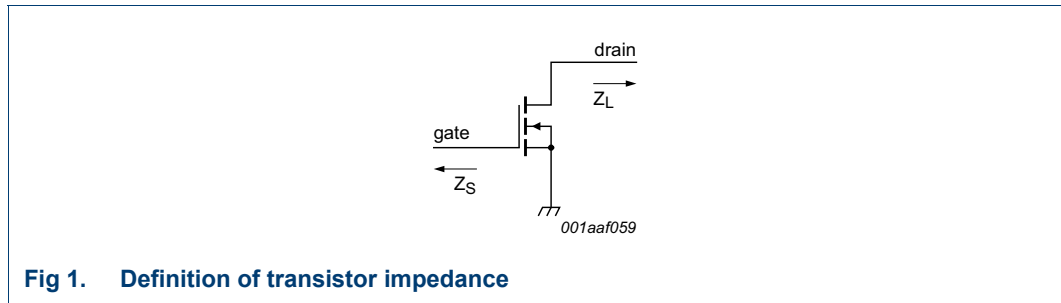
7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data per section; $V_{DS} = 28\text{ V}; I_{Dq} = 860\text{ mA}$; typical values unless otherwise specified.

f (MHz)	Z_S ^[1] (Ω)	Z_L ^[1] (Ω)
2300	4.24 – j6.5	1.5 – j5.4
2400	7.47 – j6.07	1.5 – j5.5

[1] Z_S and Z_L defined in [Figure 1](#).



7.3 Test circuit

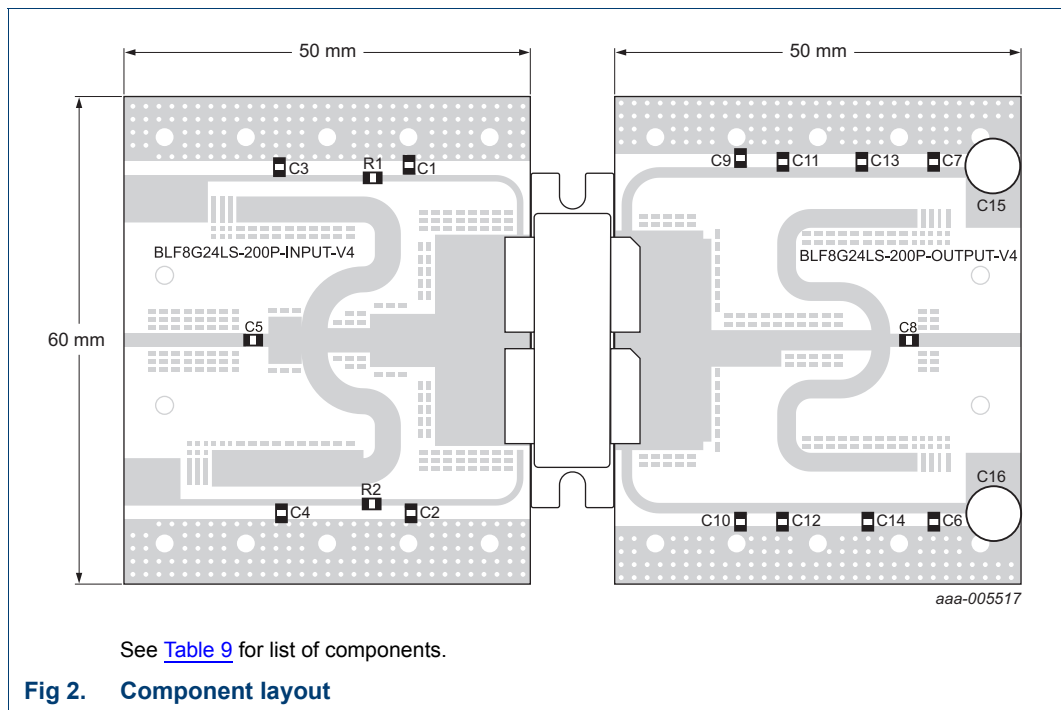


Table 9. List of components

See [Figure 2](#) for component layout.

The used PCB material is Rogers RO4350B with a thickness of 0.76 mm.

Component	Description	Value	Remarks
C1, C2, C9, C10	multilayer ceramic chip capacitor	6.8 μ F	[1]
C3, C4, C6, C7	multilayer ceramic chip capacitor	1 μ F	[2]
C5, C8	multilayer ceramic chip capacitor	33 pF	[1]
C11, C12, C13, C14	multilayer ceramic chip capacitor	0.1 μ F	[2]
C15, C16	electrolytic capacitor	1000 μ F; 50 V	
R1, R2	chip resistor	5.1 Ω	[3]

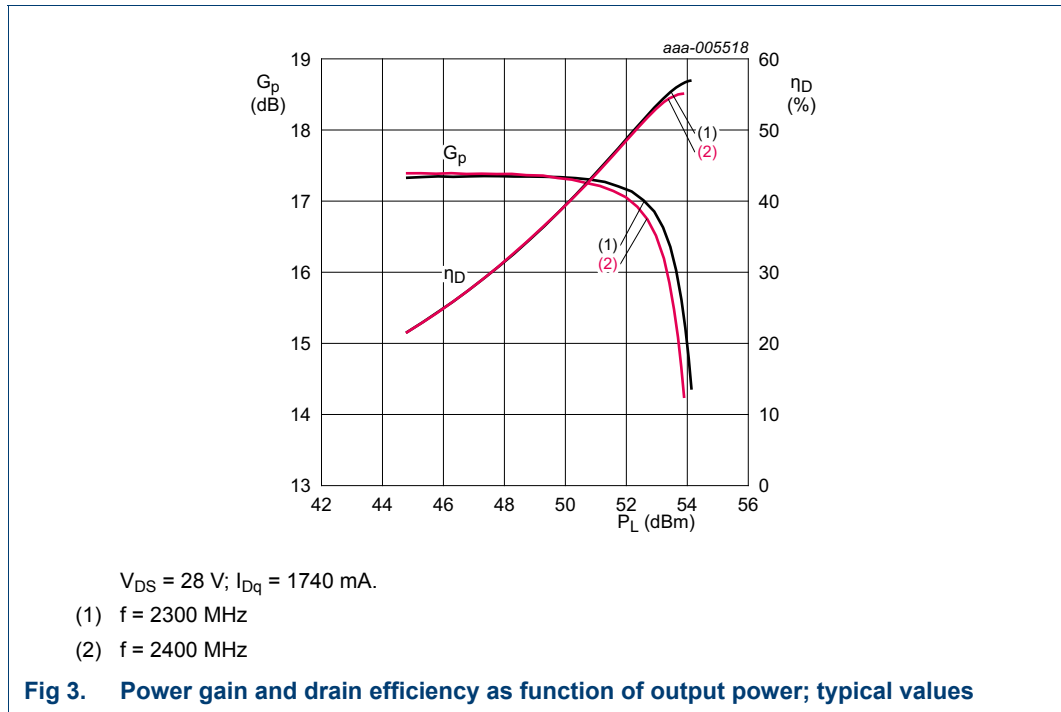
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] Murata or capacitor of same quality.

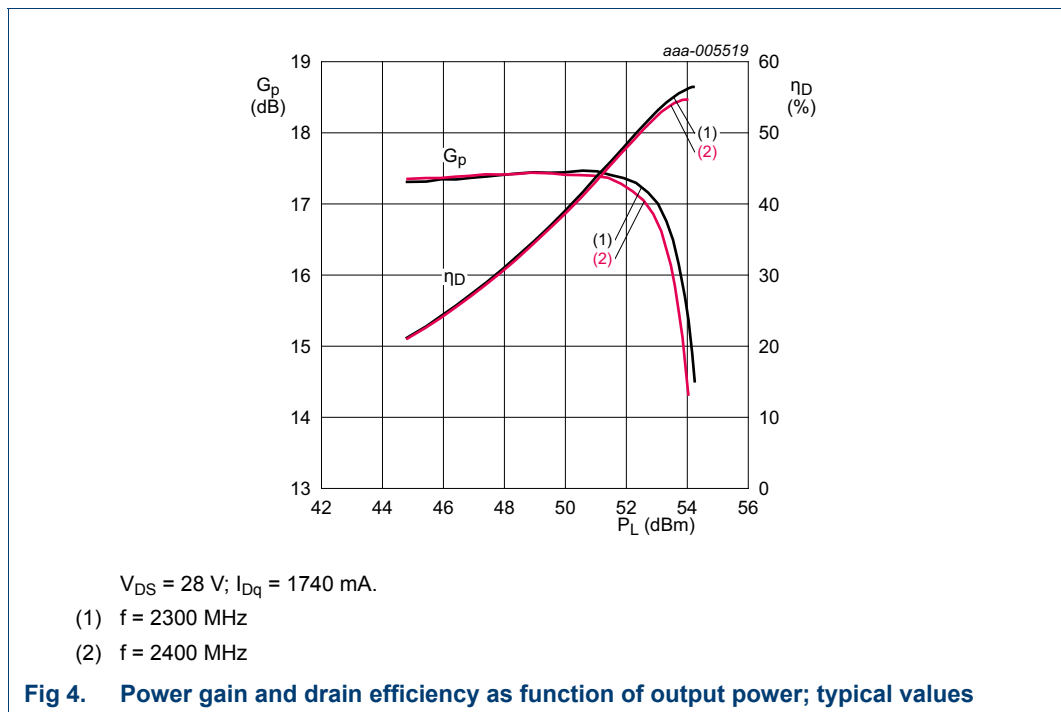
[3] Vishay Dale or resistor of same quality.

7.4 Graphical data

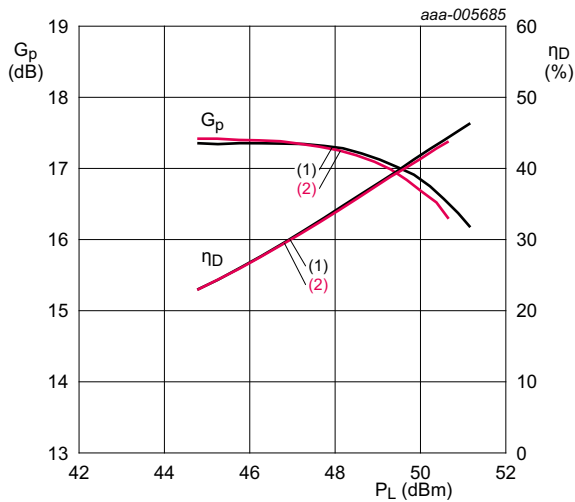
7.4.1 1-Tone CW



7.4.2 1-Tone CW pulsed

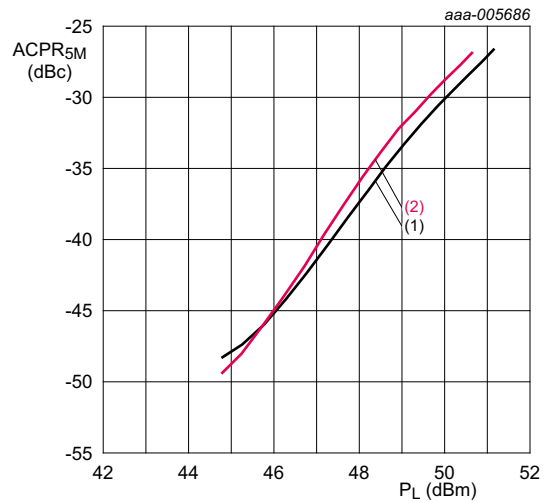


7.4.3 1-Carrier W-CDMA



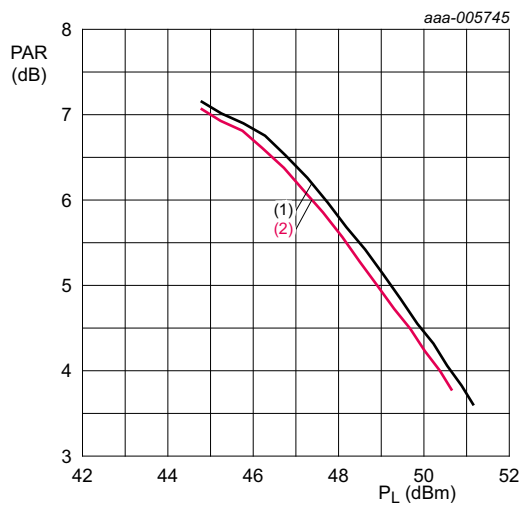
$V_{DS} = 28\text{ V}; I_{DQ} = 1740\text{ mA}$.
 (1) $f = 2300\text{ MHz}$
 (2) $f = 2400\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 28\text{ V}; I_{DQ} = 1740\text{ mA}$.
 (1) $f = 2300\text{ MHz}$
 (2) $f = 2400\text{ MHz}$

Fig 6. Adjacent power channel ratio (5 MHz) as a function of output power; typical values



$V_{DS} = 28\text{ V}; I_{DQ} = 1740\text{ mA}$.
 (1) $f = 2300\text{ MHz}$
 (2) $f = 2400\text{ MHz}$

Fig 7. Peak-to-average ratio as a function of output power; typical values

8. Package outline

Earless flanged balanced ceramic package; 4 leads

SOT539B

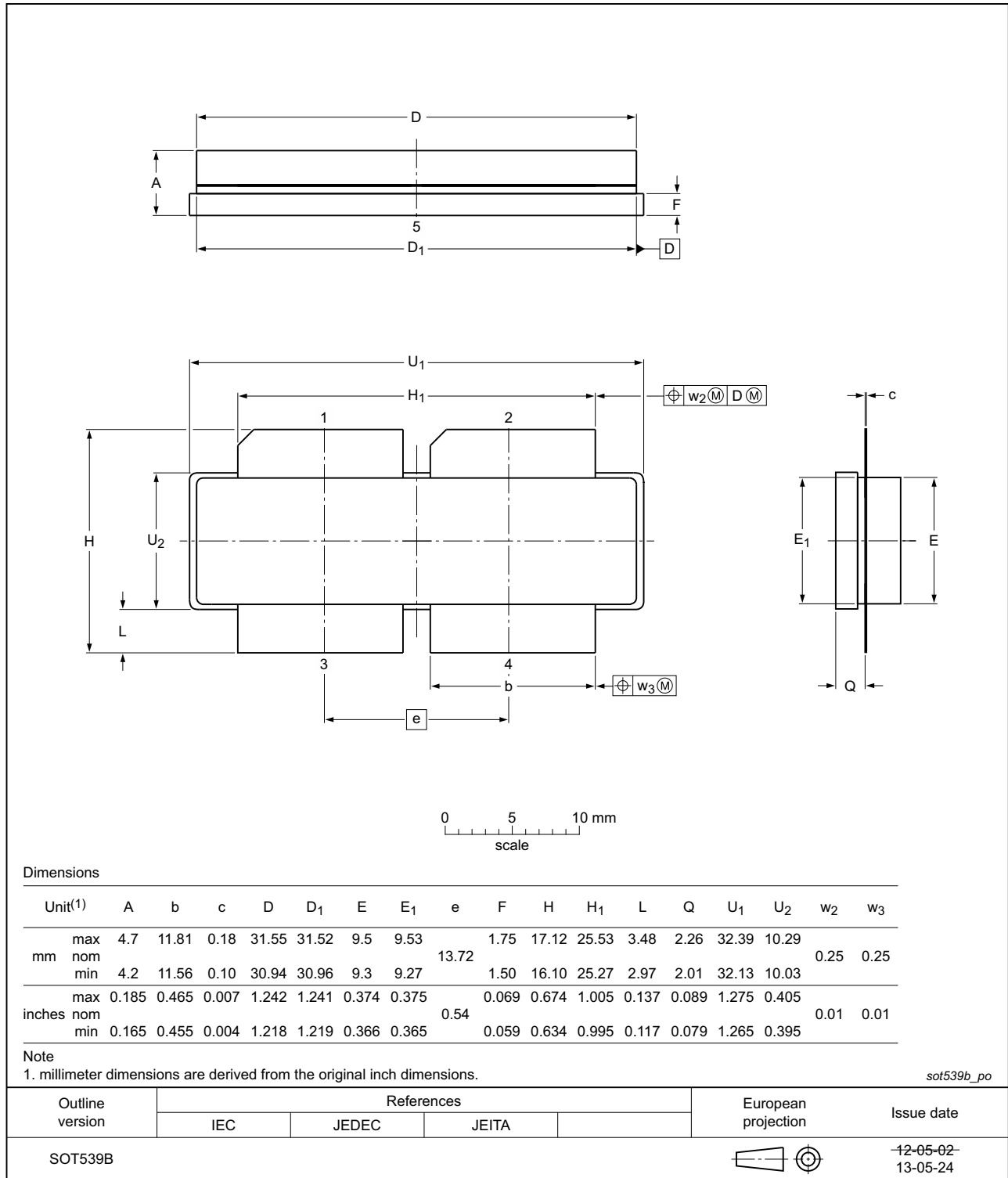


Fig 8. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical Channel
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G24LS-200PN v.3	20161201	Product data sheet	-	BLF8G24LS-200PN v.2
Modifications:	<ul style="list-style-type: none"> Section 9 on page 8: updated Handling information 			
BLF8G24LS-200PN v.2	20150901	Product data sheet	-	BLF8G24LS-200PN v.1
BLF8G24LS-200PN v.1	20140120	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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