BLL6G1214L-250

LDMOS L-band radar power transistor

Rev. 1 — 16 February 2012 | Preliminary data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C; t_p = 1 ms; δ = 10 %; I_{Dq} = 150 mA; in a class-AB production test circuit.

Test signal	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	1.2 to 1.4	36	250	15	45	15	5

1.2 Features and benefits

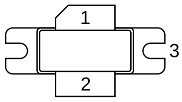
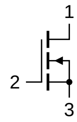
- Typical pulsed RF performance at a frequency of 1.2 GHz to 1.4 GHz, a supply voltage of 36 V, an I_{Dq} of 150 mA, a t_p of 1 ms with δ of 10 %:
  - Output power = 250 W
  - Power gain = 15 dB
  - Efficiency = 45 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6G1214L-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	89	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	59	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 85 °C; P_L = 250 W		0.244	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 250 W	[1]		
		t_p = 1000 μs; δ = 10 %		0.124	K/W
		t_p = 100 μs; δ = 10 %		0.059	K/W
		t_p = 200 μs; δ = 10 %		0.077	K/W
		t_p = 300 μs; δ = 10 %		0.088	K/W
		t_p = 100 μs; δ = 20 %		0.078	K/W

[1] $Z_{th(j-c)}$ values are calculated from results obtained with ANSYS simulations and confirmed with IR measurements during development stage. During production: guaranteed by design.

6. Characteristics

Table 6. DC Characteristics

T_j = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.36 mA	91.5	-	105.5	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 336 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 42 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	50	59	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 336 mA	51.6	-	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 11.7 A	-	-	127	mΩ
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 40 V; f = 1 MHz	-	285	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 40 V; f = 1 MHz	-	90	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 40 V; f = 1 MHz	-	3	-	pF

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 1 ms; δ = 10 %; RF performance at V_{DS} = 36 V; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	-	36	V
I_{Dq}	quiescent drain current	No RF applied	-	150	-	mA
P_L	output power		250	-	-	W
f_{range}	frequency range		1200	-	1400	MHz
t_p	pulse duration	δ = 10 %	-	-	1	ms
		δ = 20 %	-	-	100	μs

Table 7. RF characteristics *…continued*

Test signal: pulsed RF; t_p = 1 ms; δ = 10 %; RF performance at V_{DS} = 36 V; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
η_D	drain efficiency			42	45	-	%
t_r	rise time	P_L = 250 W	[1]	-	-	200	ns
t_f	fall time	P_L = 250 W	[1]	-	-	200	ns
G_p	power gain			13	15	-	dB
$P_{droop(pulse)}$	pulse droop power			-	-	0.6	dB
RL_{in}	input return loss			-	-	−8	dB

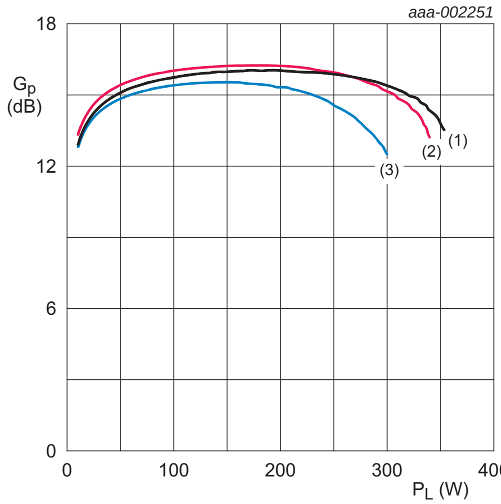
[1] The rise and fall time of the input circuit will be 5 ns maximum.

6.1 Ruggedness in class-AB operation

The BLL6G1214L-250 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 36 V; I_{Dq} = 150 mA; P_L = 250 W; t_p = 1 ms; δ = 10 %.

7. Application information

7.1 Graphs



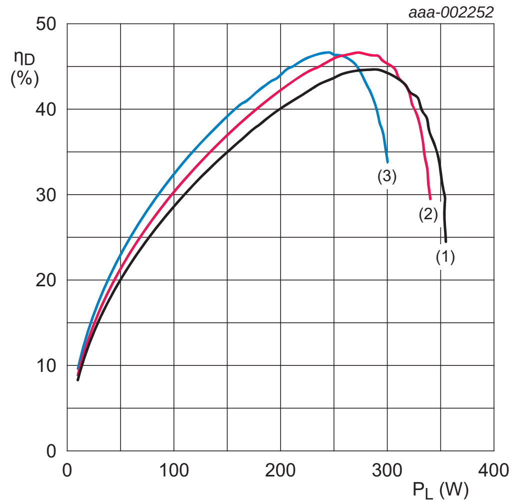
t_p = 100 μs; δ = 10 %; T_h = 25 °C.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 1. Power gain as a function of output power; typical values



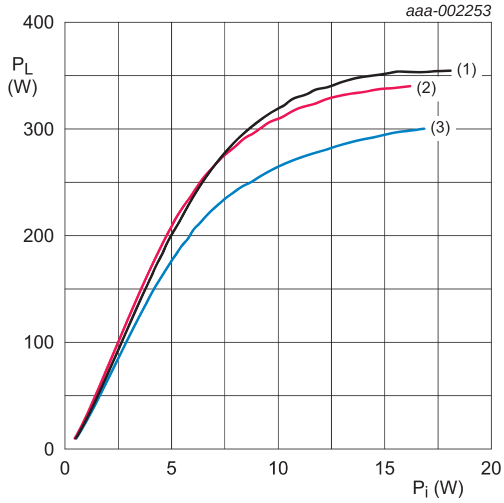
t_p = 100 μs; δ = 10 %; T_h = 25 °C.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 2. Drain efficiency as a function of output power; typical values



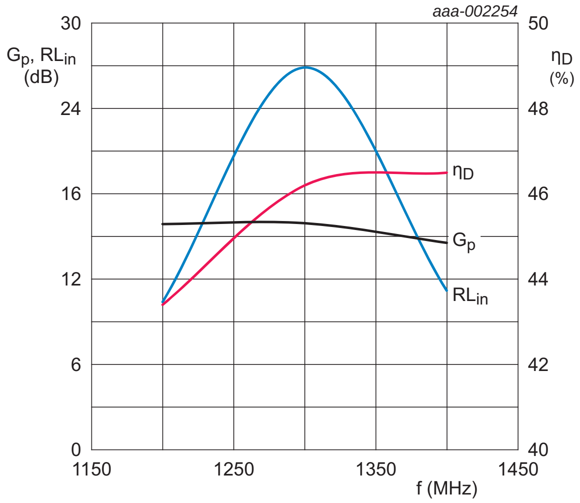
t_p = 100 μs; δ = 10 %; T_h = 25 °C.

(1) f = 1200 MHz

(2) f = 1300 MHz

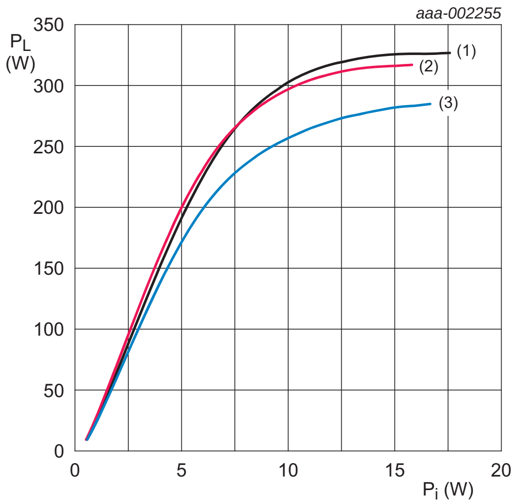
(3) f = 1400 MHz

Fig 3. Output power as a function of input power; typical values



P_L = 250 W; t_p = 100 μs; δ = 10 %; T_h = 25 °C.

Fig 4. Power gain, input return loss and drain efficiency as function of frequency; typical values



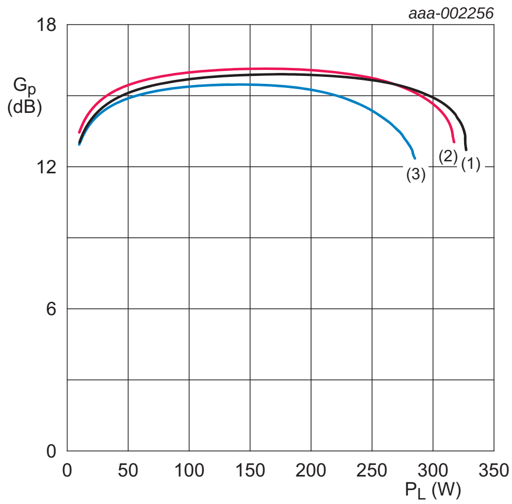
t_p = 1 ms; δ = 10 %; T_h = 25 °C.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 5. Output power as a function of input power; typical values



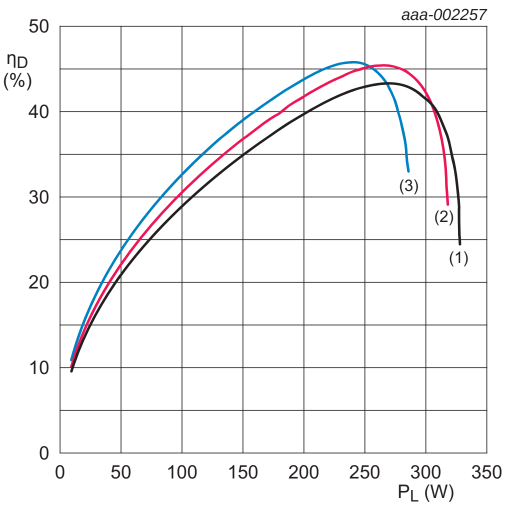
t_p = 1 ms; δ = 10 %; T_h = 25 °C.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 6. Power gain as a function of output power; typical values



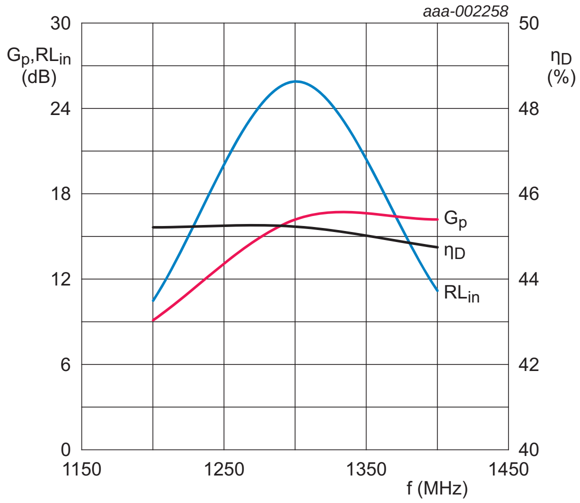
t_p = 1 ms; δ = 10 %; T_h = 25 °C.

(1) f = 1200 MHz

(2) f = 1300 MHz

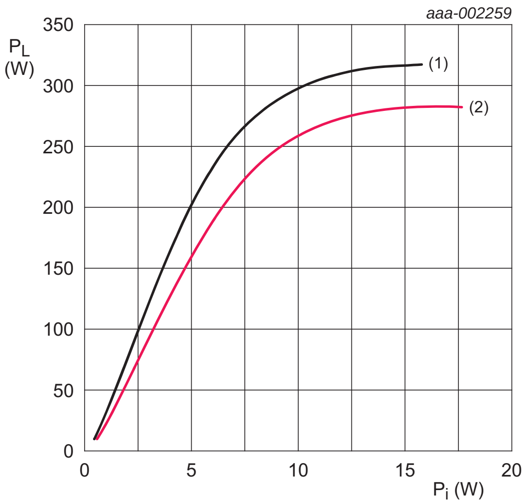
(3) f = 1400 MHz

Fig 7. Drain efficiency as a function of output power; typical values



P_L = 250 W; t_p = 1 ms; δ = 10 %; T_h = 25 °C.

Fig 8. Power gain, input return loss and drain efficiency as function of frequency; typical values

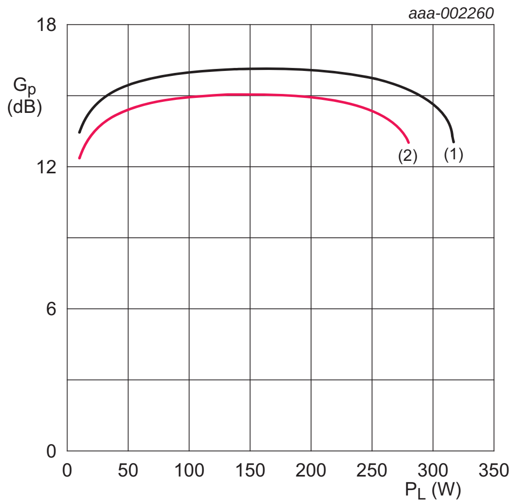


f = 1300 MHz; t_p = 1 ms; δ = 10 %.

(1) T_h = 25 °C

(2) T_h = 85 °C

Fig 9. Output power as a function of input power; typical values

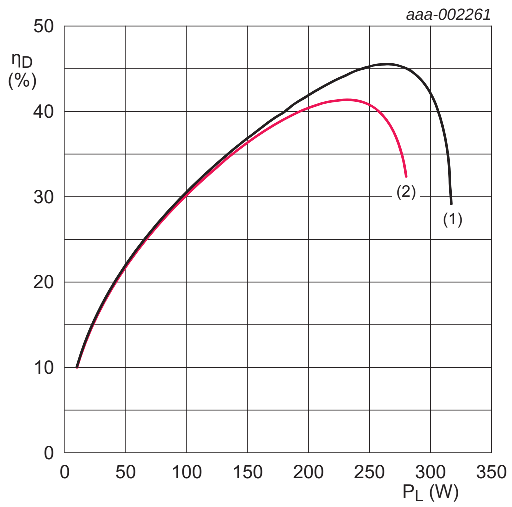


f = 1300 MHz; t_p = 1 ms; δ = 10 %.

(1) T_h = 25 °C

(2) T_h = 85 °C

Fig 10. Power gain as a function of output power; typical values

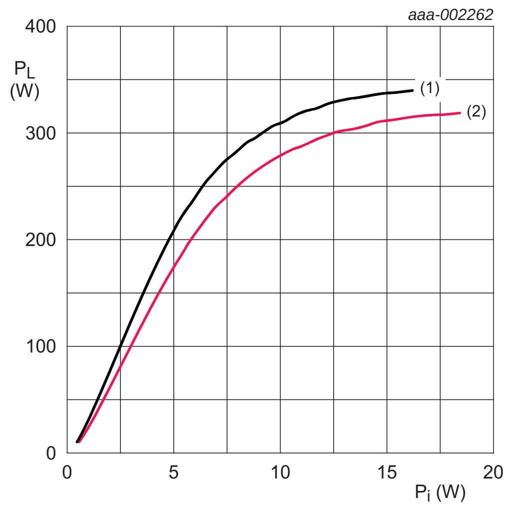


f = 1300 MHz; t_p = 1 ms; δ = 10 %.

(1) T_h = 25 °C

(2) T_h = 85 °C

Fig 11. Drain efficiency as a function of output power; typical values

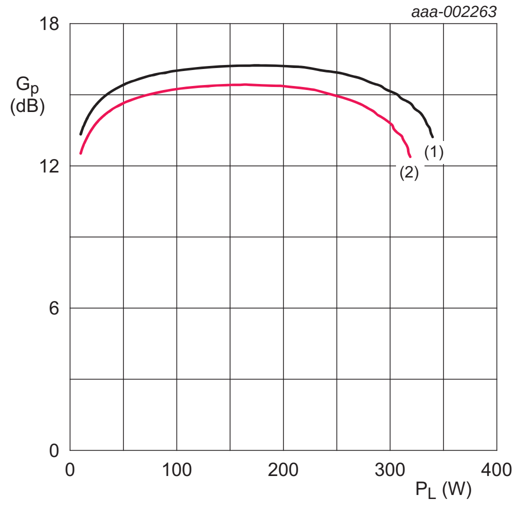


f = 1300 MHz; t_p = 100 μs; δ = 10 %.

(1) T_h = 25 °C

(2) T_h = 85 °C

Fig 12. Output power as a function of input power; typical values

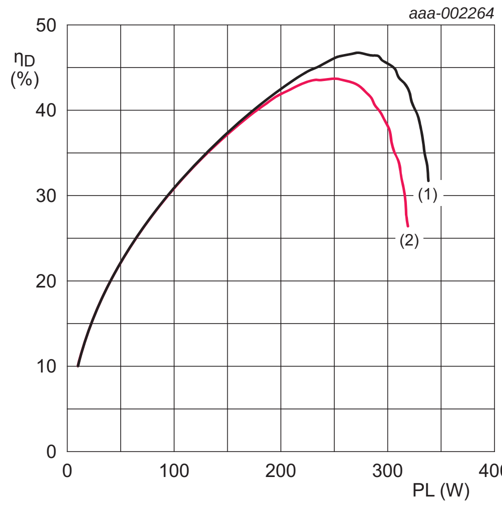


f = 1300 MHz; t_p = 1 ms; δ = 10 %.

(1) T_h = 25 °C

(2) T_h = 85 °C

Fig 13. Power gain as a function of output power; typical values



f = 1300 MHz; t_p = 100 μs; δ = 10 %.

(1) T_h = 25 °C

(2) T_h = 85 °C

Fig 14. Drain efficiency as a function of output power; typical values

7.2 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f GHz	Z_S Ω	Z_L Ω
1.2	1.077 – j2.78	1.288 – j1.014
1.3	1.352 – j2.949	1.139 – j1.086
1.4	1.881 – j2.640	1.038 – j1.132

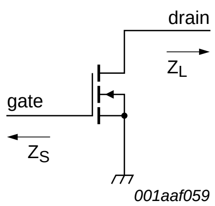
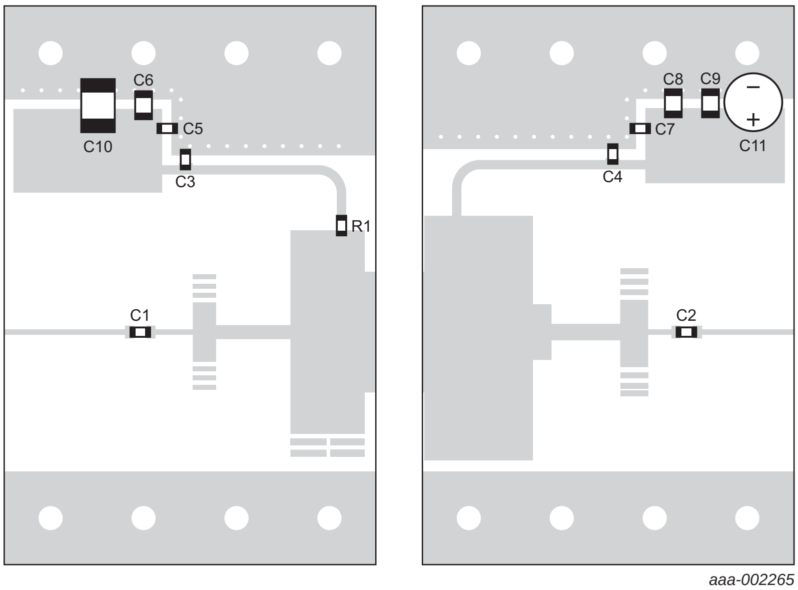


Fig 15. Definition of transistor impedance

7.3 Circuit information



Printed-Circuit Board (PCB): Duroid 6010; ε_r = 10.15; thickness = 0.64 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 16. Component layout for application circuit

Table 9. List of components

For test circuit see Figure 16.

Component	Description	Value		Remarks
C1, C2, C3, C4, C7	multilayer ceramic chip capacitor	56 pF	[1]	
C5, C8	multilayer ceramic chip capacitor	200 pF	[2]	
C6, C9	multilayer ceramic chip capacitor	1 nF	[3]	
C10	multilayer ceramic chip capacitor	10 μF; 20 V		
C11	electrolytic capacitor	22 μF; 63 V		
R1	SMD resistor	10 Ω		0603

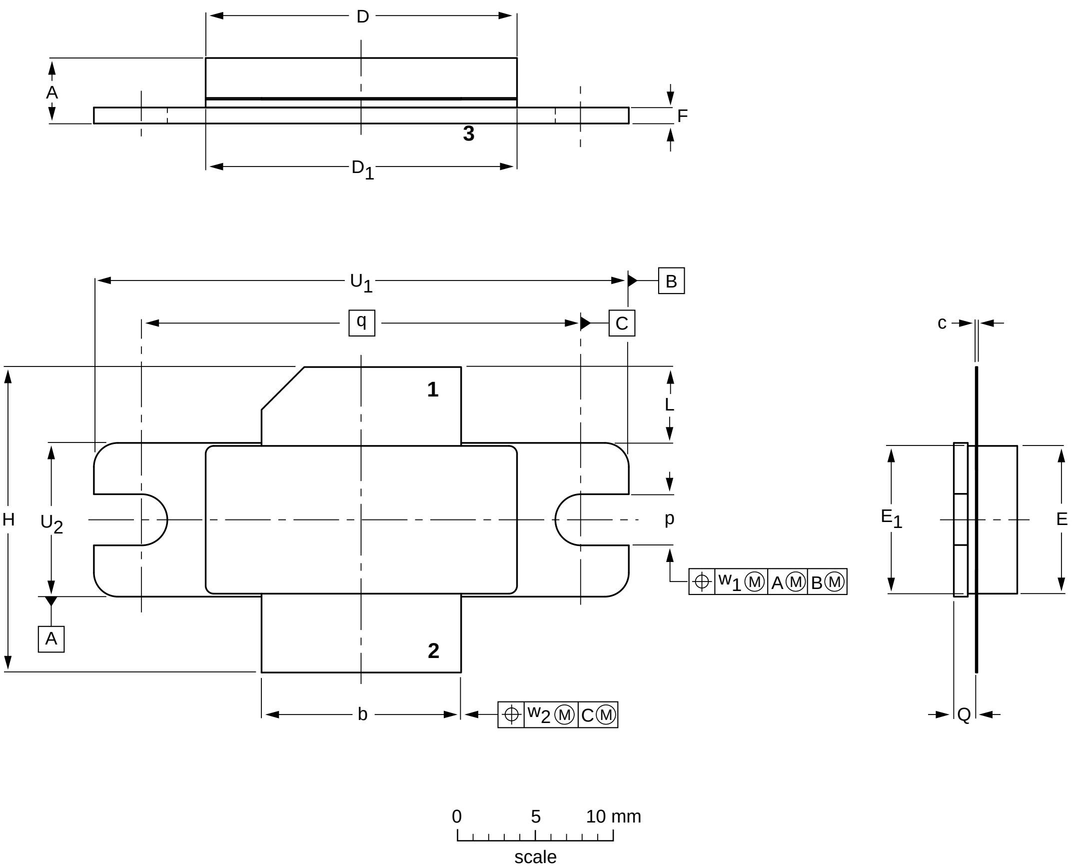
[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 700A or capacitor of same quality.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 17. Package outline SOT502A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
DC	Direct Current
ESD	ElectroStatic Discharge
IR	InfraRed
L-band	Long wave band
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6G1214L-250 v.1	20120216	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1 Product profile . . . 1
1.1 General description . . . 1
1.2 Features and benefits . . . 1
1.3 Applications . . . 1
2 Pinning information . . . 2
3 Ordering information . . . 2
4 Limiting values . . . 2
5 Thermal characteristics . . . 3
6 Characteristics . . . 3
6.1 Ruggedness in class-AB operation . . . 4
7 Application information . . . 4
7.1 Graphs . . . 4
7.2 Impedance information . . . 8
7.3 Circuit information . . . 8
8 Package outline . . . 10
9 Handling information . . . 11
10 Abbreviations . . . 11
11 Revision history . . . 11
12 Legal information . . . 12
12.1 Data sheet status . . . 12
12.2 Definitions . . . 12
12.3 Disclaimers . . . 12
12.4 Trademarks . . . 13
13 Contact information . . . 13
14 Contents . . . 14

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