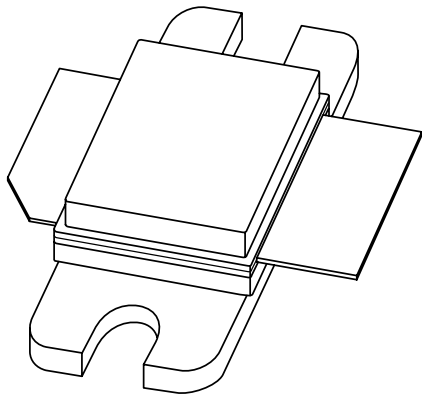


DATA SHEET



BLS2731-110

Microwave power transistor

Product specification
Supersedes data of 1998 Jan 30

2001 Dec 05

Microwave power transistor

BLS2731-110

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

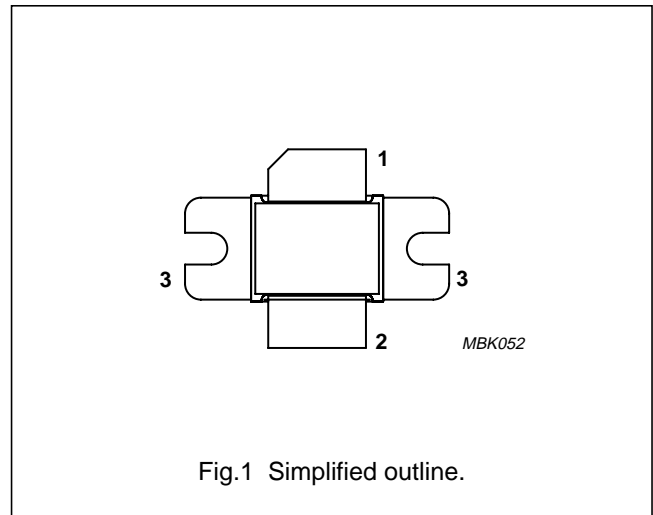
- Common base class-C pulsed power amplifiers for radar applications in the 2.7 to 3.1 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT423A) with the common base connected to the flange.

PINNING - SOT423A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange



QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^\circ\text{C}$ in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_c (%)
Pulsed class-C	2.7 to 3.1	40	>110	>7	>35

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100 \mu\text{s}; \delta \leq 10\%$	–	12	A
P_{tot}	total power dissipation	$t_p = 100 \mu\text{s}; \delta = 10\%; T_{mb} = 25 \text{ }^\circ\text{C}$	–	500	W
T_{stg}	storage temperature		–65	+200	$^\circ\text{C}$
T_j	operating junction temperature		–	200	$^\circ\text{C}$
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10 \text{ s}$	–	235	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j-h}$	thermal impedance from junction to heatsink	$t_p = 100 \mu\text{s}; \delta = 10\%$; note 1	0.24	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS $T_j = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

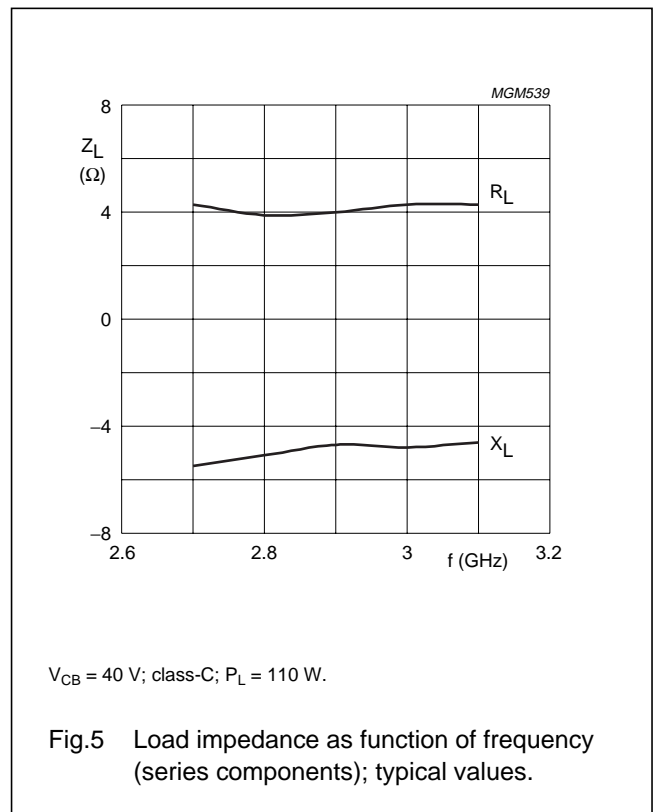
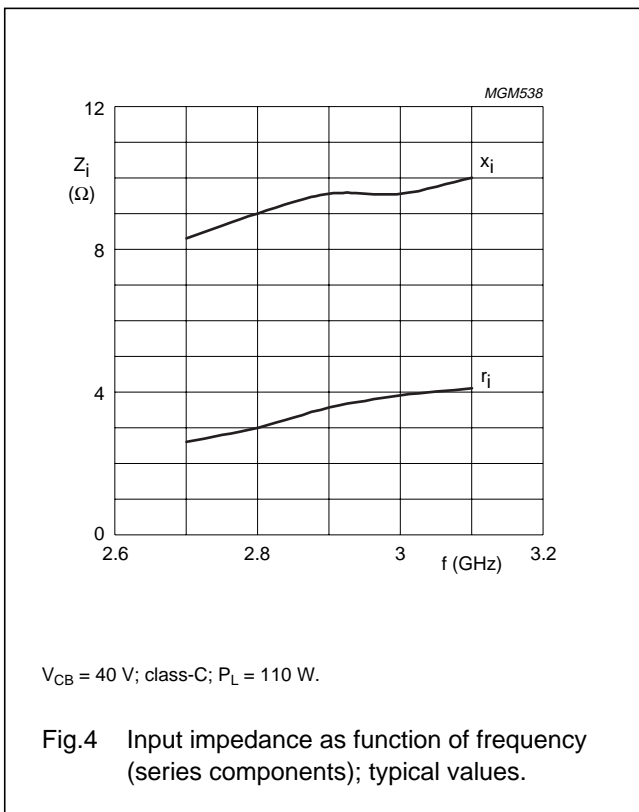
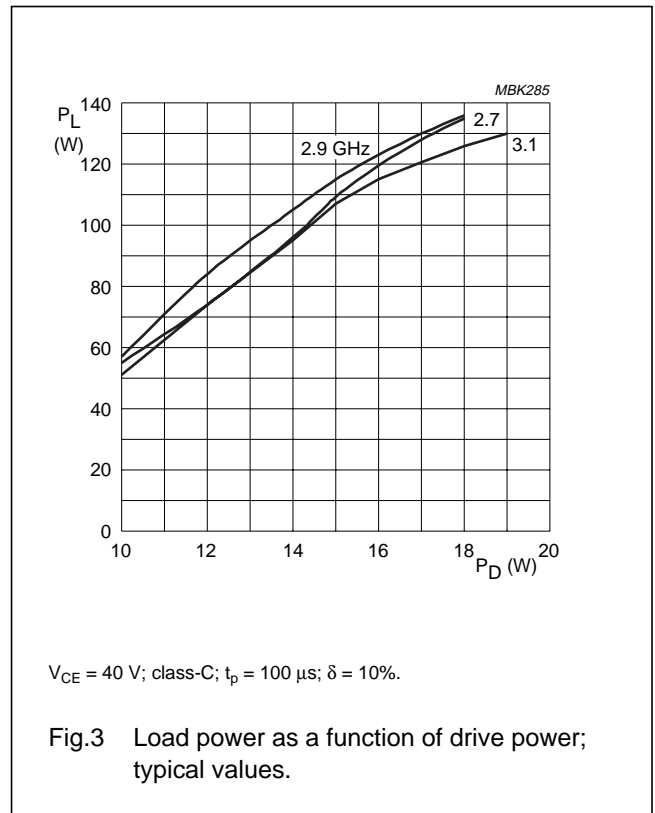
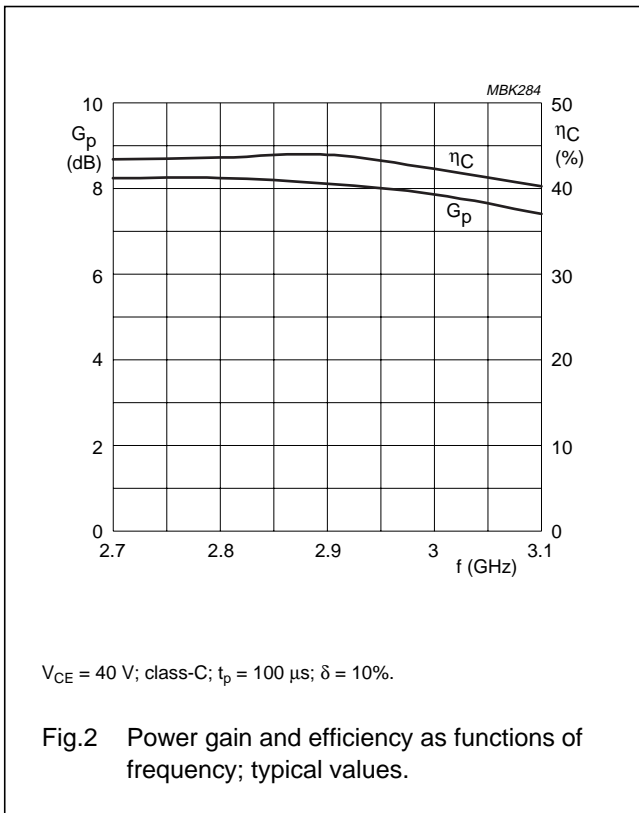
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 30 \text{ mA}$; open emitter	75	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 30 \text{ mA}$; $V_{BE} = 0$	75	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40 \text{ V}$; $I_E = 0$	–	3	mA
I_{CES}	collector leakage current	$V_{CE} = 40 \text{ V}$; $V_{BE} = 0$	–	6	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5 \text{ V}$; $I_C = 0$	–	0.6	mA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}$; $I_C = 3 \text{ A}$	40	100	

APPLICATION INFORMATIONRF performance at $T_h = 25 \text{ }^\circ\text{C}$ in a common base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)
Class-C; $t_p = 100 \mu\text{s}; \delta = 10\%$	2.7 to 3.1	40	≥ 110	≥ 7	≥ 35
	2.7 to 2.9	40	typ. 130	typ. 8	typ. 42
	2.9 to 3.1	40	typ. 120	typ. 7.5	typ. 40

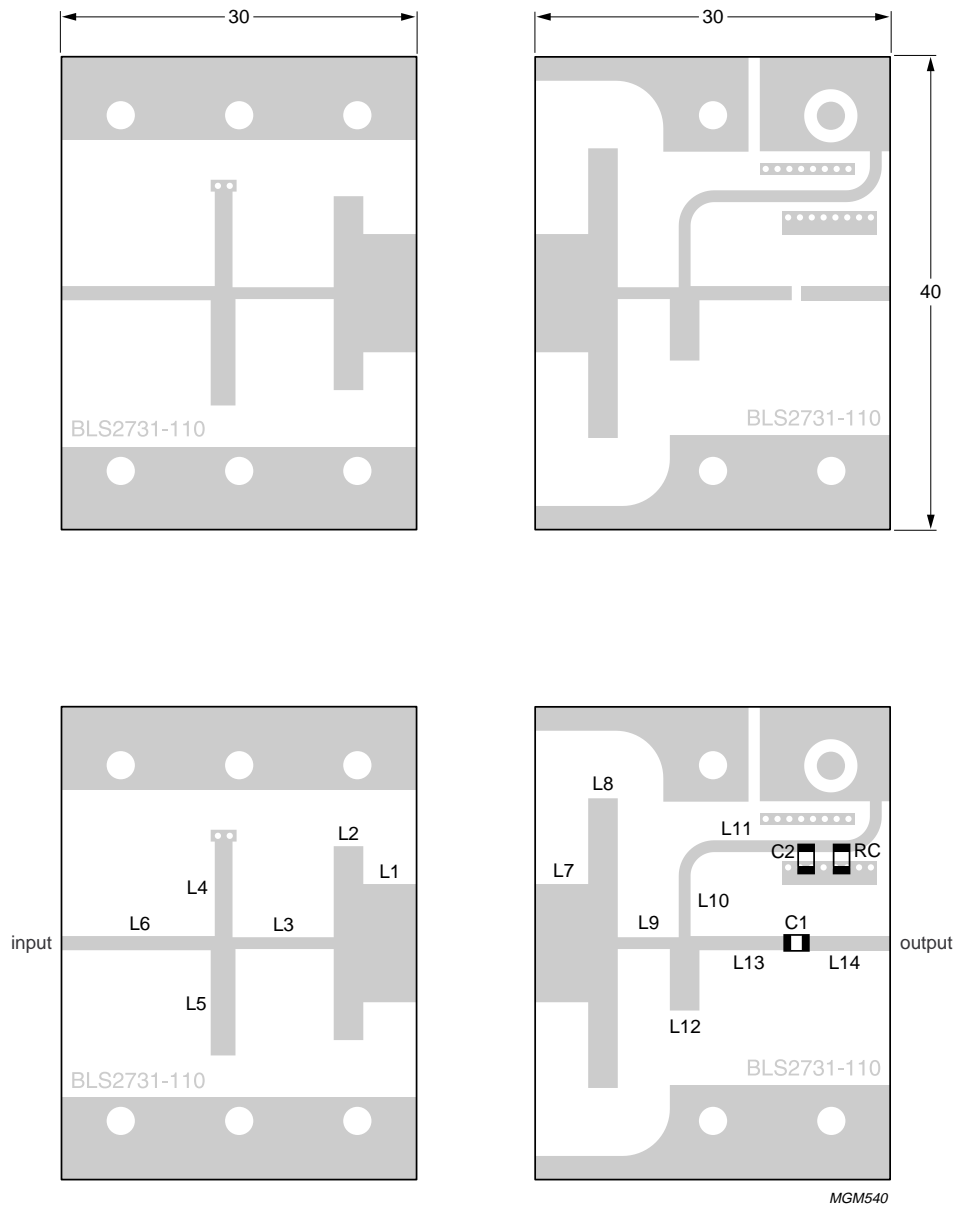
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Dimensions in mm.

The components are located on one side of the copper-clad printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.6 Component layout for 2.7 to 3.1 GHz class-C test circuit.

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List of components (see Fig.6)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor; note 1	12 pF	
C2	multilayer ceramic chip capacitor; note 1	18 pF	
RC	multilayer ceramic chip capacitor in series with SMD resistor	100 nF + 5 Ω	
L1	stripline; note 2		length 4.5 mm width 10 mm
L2	stripline; note 2		length 2.5 mm width 16.4 mm
L3	stripline; note 2		length 8.3 mm width 1 mm
L4	stripline; note 2		length 8 mm width 1.5 mm
L5	stripline; note 2		length 2 mm width 8.9 mm
L6	stripline; note 2		length 12.7 mm width 1.2 mm
L7	stripline; note 2		length 4.5 mm width 10 mm
L8	stripline; note 2		length 2.5 mm width 24.4 mm
L9	stripline; note 2		length 4.4 mm width 1 mm
L10	stripline; note 2		length 5.2 mm width 1 mm
L11	stripline; note 2		length 9.3 mm width 1 mm
L12	stripline; note 2		length 2.5 mm width 6 mm
L13	stripline; note 2		length 7.8 mm width 1.2 mm
L14	stripline; note 2		length 7.5 mm width 1.2 mm

Notes

- American Technical Ceramics type 100A or capacitor of same quality.
- The striplines are on double-clad printed-circuit board with Duroid dielectric ($\epsilon_r = 2.2$); thickness = 0.38 mm.

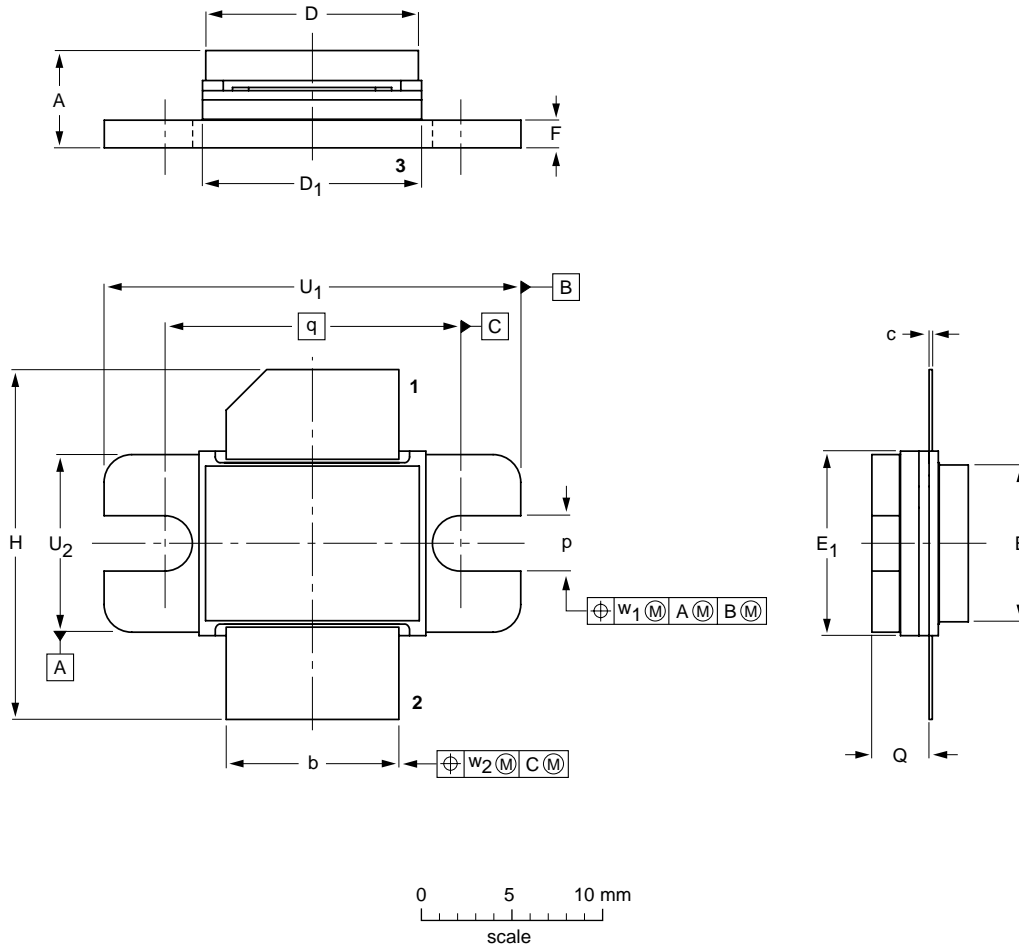
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PACKAGE OUTLINE

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT423A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	5.72 4.90	9.53 9.27	0.10 0.05	12.09 11.71	12.83 12.57	8.84 8.56	10.29 10.03	1.58 1.47	19.81 18.29	3.43 3.18	3.35 2.95	16.51	22.99 22.73	9.91 9.65	0.25	0.76
inches	0.225 0.193	0.375 0.365	0.004 0.002	0.476 0.461	0.505 0.495	0.348 0.337	0.405 0.395	0.062 0.058	0.78 0.72	0.135 0.125	0.132 0.116	0.65	0.905 0.895	0.390 0.380	0.01	0.03

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT423A					99-03-29

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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NOTES

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NOTES

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NOTES

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